Theory of Semiconductor Devices
(반도체 소자 이론)

Lecture 21

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Bipolar Transistor

-5.1 INTRODUCTION

- A ***transistor***, derived from transfer resistor, is a ***three***-terminal device whose resistance between two terminals is ***controlled*** by the third.

- The ***bipolar transistor***, one of the most-important semiconductor devices, was invented by a research team at Bell Laboratories in 1947. It has had an unprecedented impact on the electronic industry in general and on solid-state research in particular.

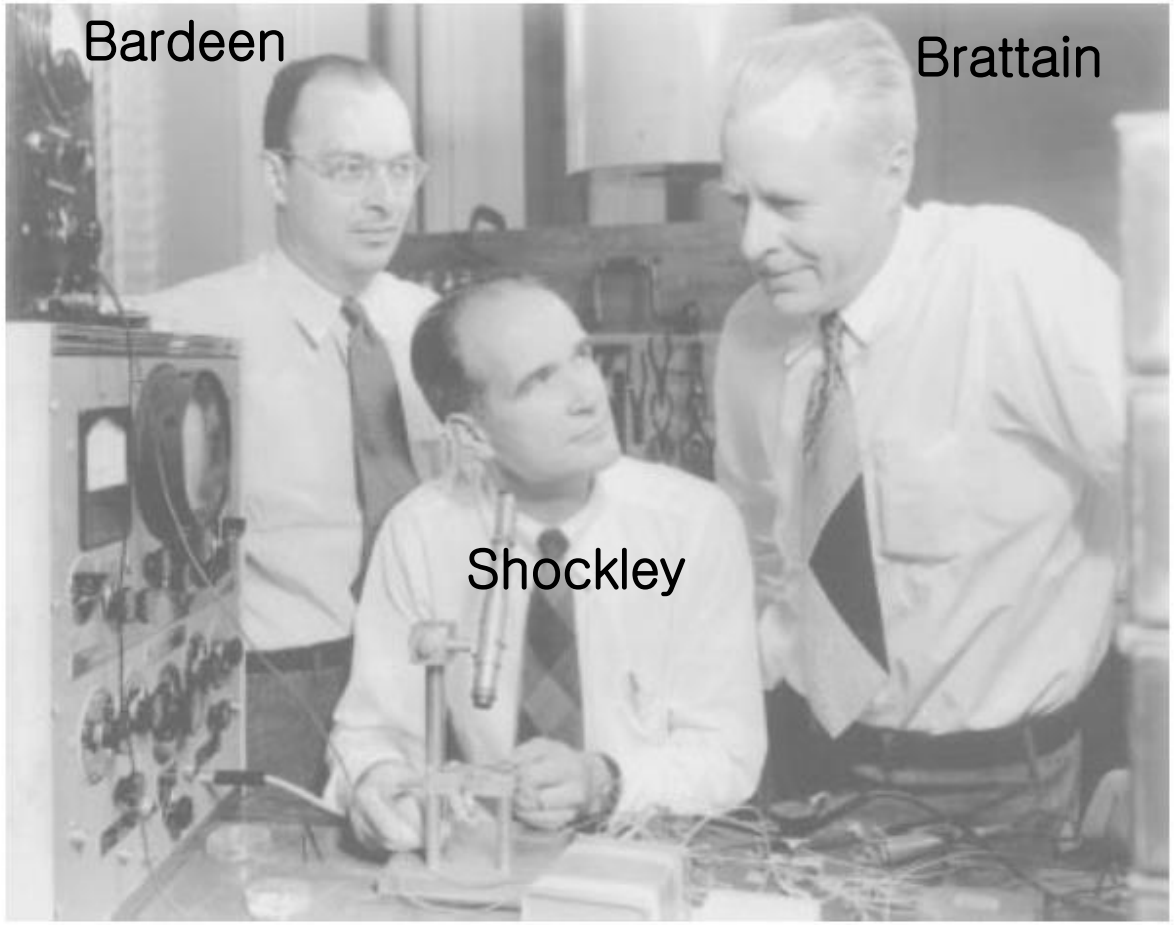
- Prior to 1947 semiconductors were only used as thermistors, photodiodes, and rectifiers, all ***two***-terminal devices.

- In 1948 **Bardeen** and **Brattain** made the announcement of new experimental observation on the point-contact transistor.
-In the following year **Shockley**'s classic paper on junction diodes and transistors was published. The theory of minority-carrier injection of ***p-n*** junctions forms the basis of the junction transistor.

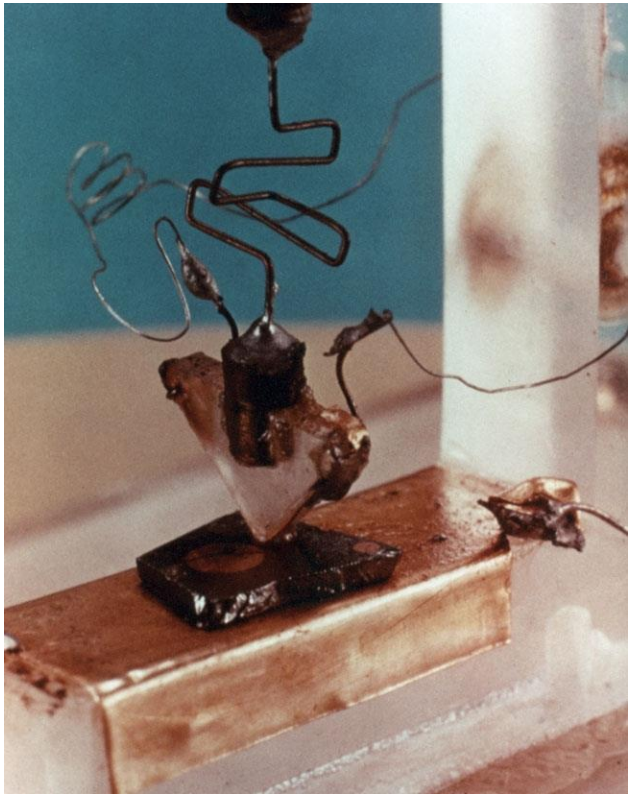
- The first junction bipolar transistor was demonstrated in 1951.

Inventors of the Transistor

Bardeen, Shockley, and Brattain



Nobel Prize (Physics) @1956



The first point-contact Transistor invented.

Bell Telephone Lab.
Dec. 23, 1947

Bipolar Transistor

- Since then the transistor theory has been extended to include high-frequency, high-power, and switching behaviors.
- Many breakthroughs have been made in transistor technology, particularly in the areas of ***crystal growth***, ***epitaxy*** , ***diffusion, ion implantation*** , ***lithography*** , ***dry etch*** , ***surface passivation*** , ***planarization*** , and ***multilevel metallization***.
- These breakthroughs have helped increase the power and frequency capabilities as well as the reliability of transistors.

- The bipolar transistor is now a key element, for example, in some high-speed computers, in vehicles and satellites, and in modern communication and power systems.

5.2 STATIC CHARACTERISTICS

5.2.1 Basic Current-Voltage Relationship

-In this section we consider the ***basic dc characteristics*** of a bipolar transistor. **Figure 1** shows the symbols and nomenclatures for *n-p-n* and *p-n-p* transistors. The arrow indicates the direction of current flow under ***normal*** operating condition, that is, *forward* biased emitter junction and *reverse*-biased collector junction.
-A bipolar transistor can be connected in three circuit configurations, depending on which lead is common to the input and output circuits.

Bipolar Transistor

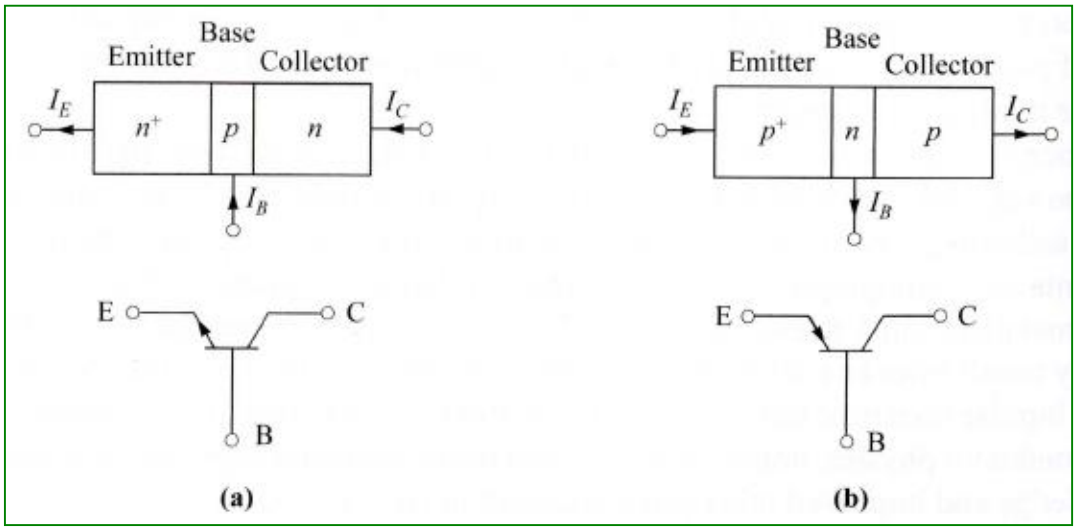


Fig.l Symbols and nomenclatures of
(a) *n-p-n* transistors and
(b) *p-n-p* transistors.

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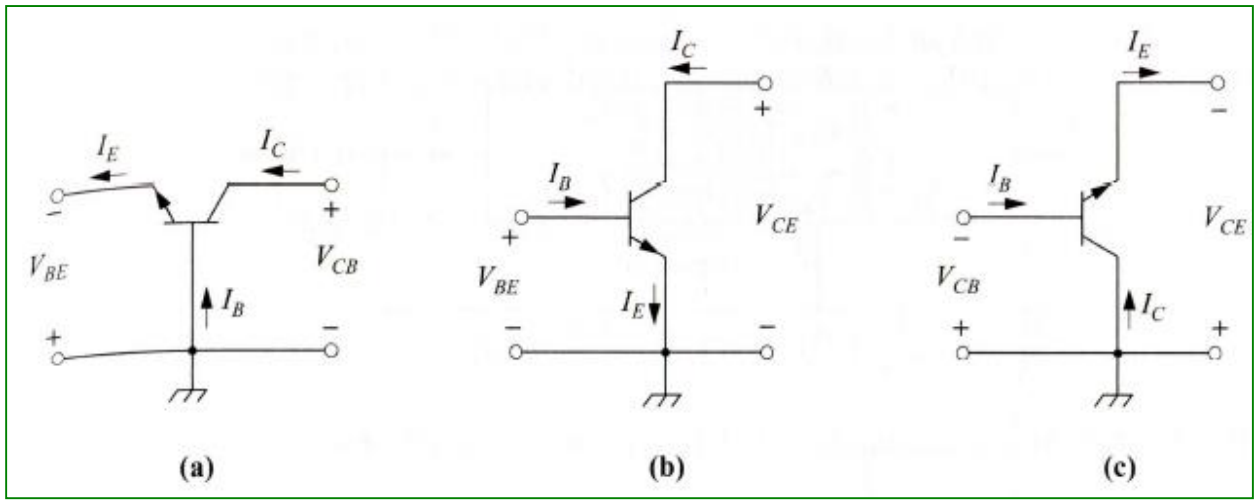
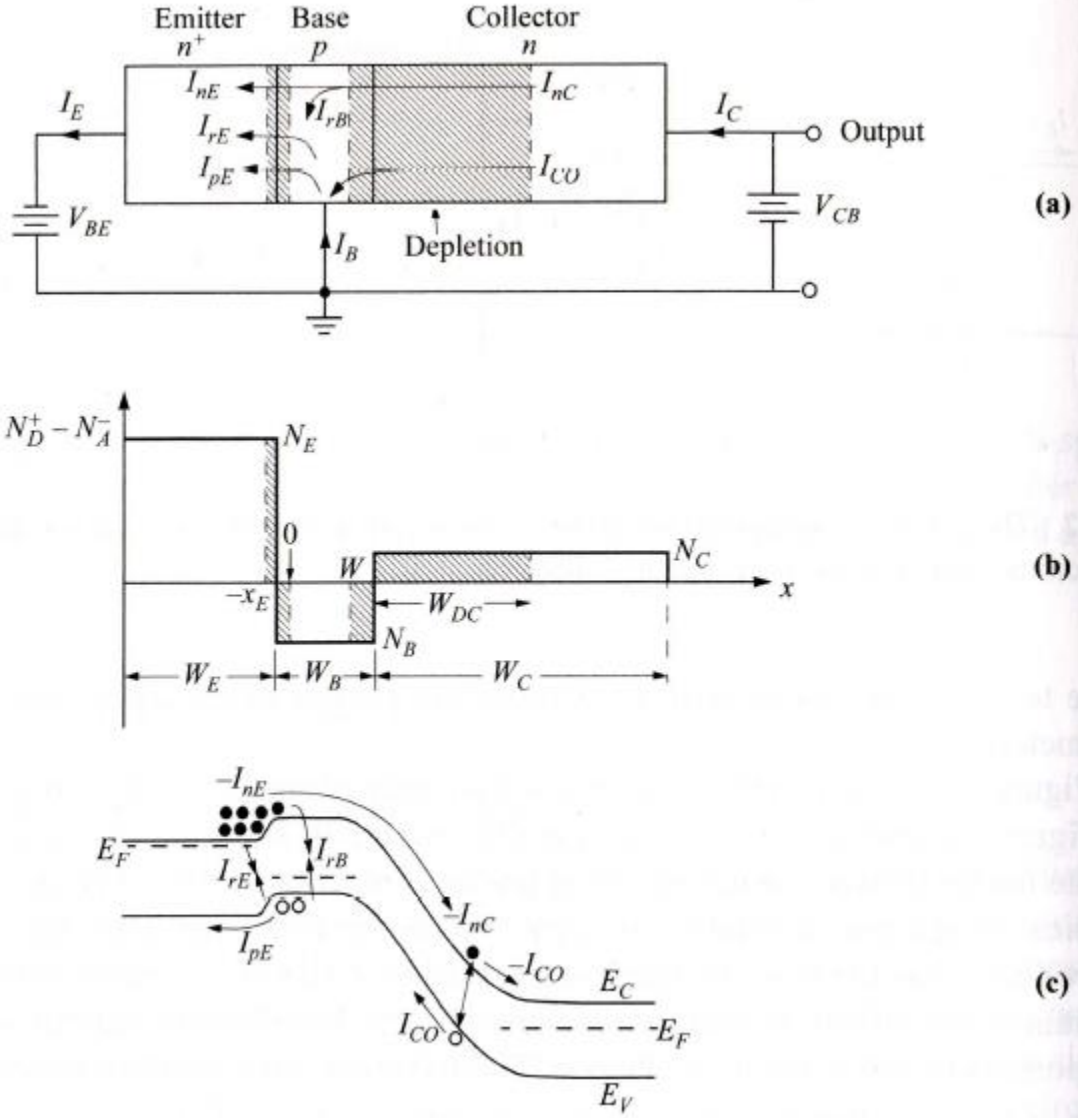


Fig. 2 Three biasing configurations of *n-p-n* transistors in normal mode:
(a) common-base,
(b) common-emitter, and
(c) common-collector.

Bipolar Transistor



- **Figure 3**a is a schematic of an *n-p-n* transistor connected in the ***common-base*** configuration and biased in normal mode.

Fig. 3

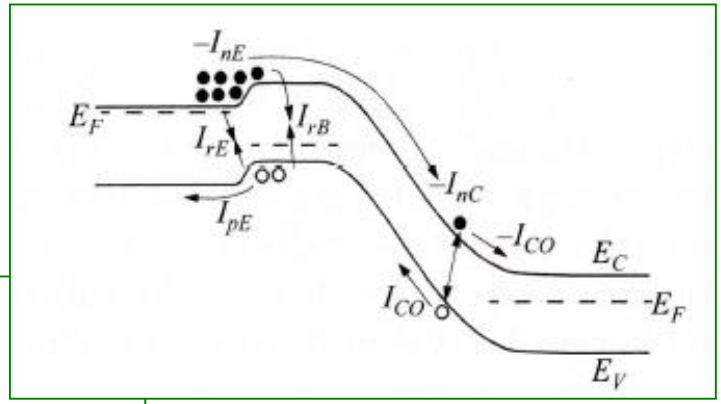
An *n-p-n* transistor biased in the normal operating conditions.
(a) Connection and biases in ***common-base*** configuration.
(b) Doping profiles and critical dimensions with abrupt impurity distributions.
(c) Energy-band diagram. Current components are shown in (a) and (c).

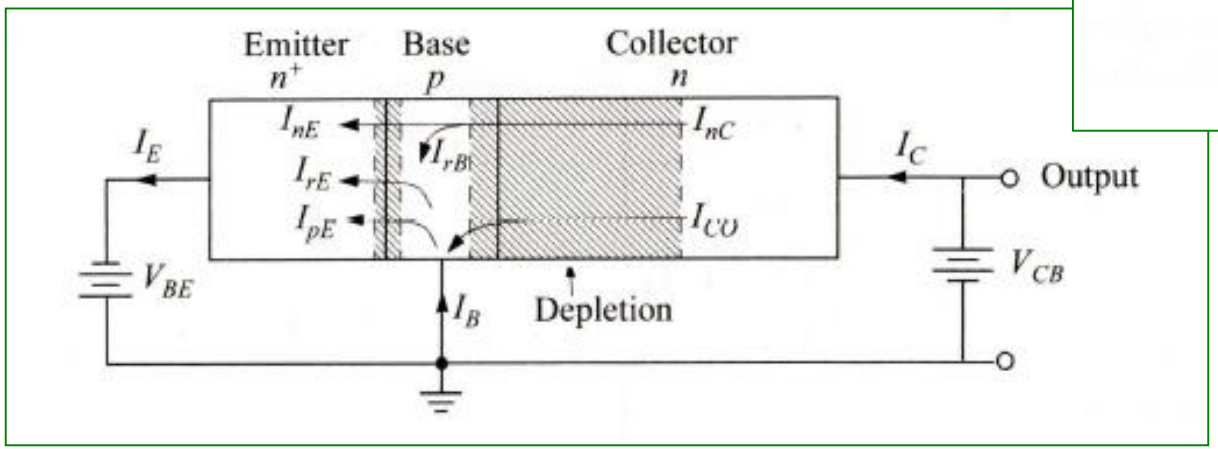
Note that in (c), flow of electrons is negative current because of negative charge.

Bipolar Transistor

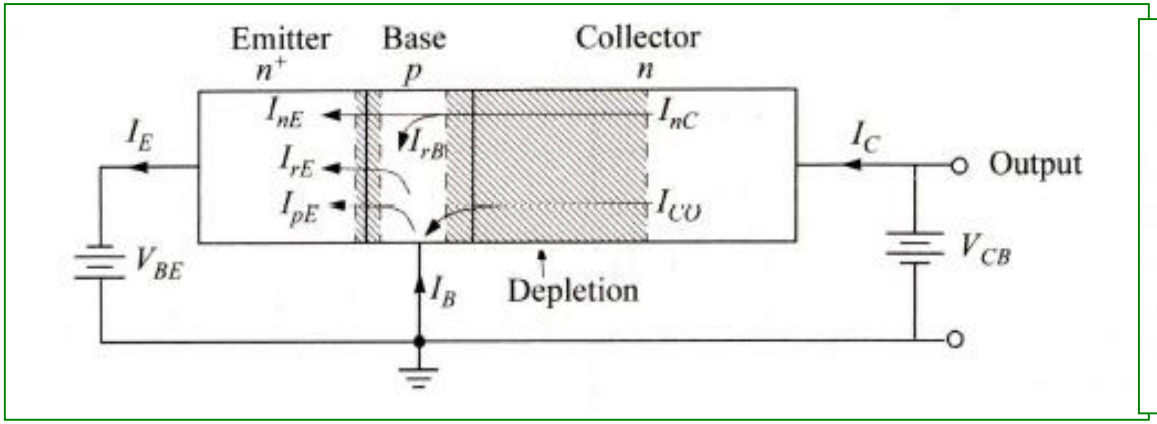
- **Figures 3**a and b also indicate all ***current*** components biased under *normal* mode. These currents are explained below:

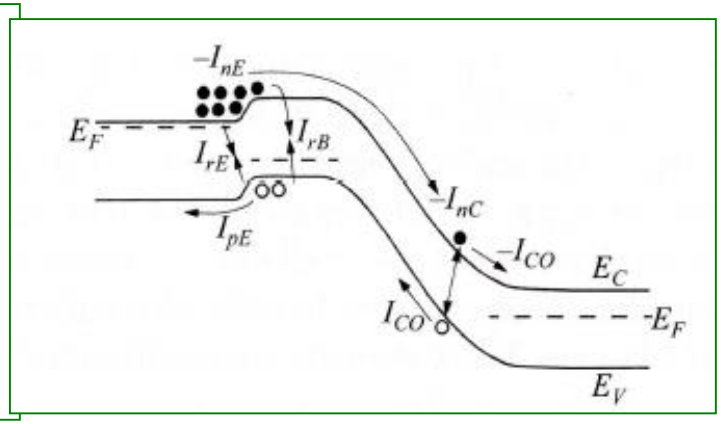
I_{nE} : Electron **diffusion** current injected at emitter-base junction.
I_{nC} : Electron **diffusion** current reaching the collector.
I_{rB} : (= I_{nE} - I_{nC}) Loss of electron current **recombining** in the base.
I_{pE} : Hole **diffusion** current at emitter-base junction.
I_{rE} : **Recombination** current at emitter-base junction.
I_{CO} : **Reverse** current at collector-base junction.





Bipolar Transistor





- The ***basic operation*** of a bipolar transistor can be explained ***qualitatively***, considering first only the *major* current components.

(1) When the emitter-base junction is *forward* biased, the *p*-*n* junction current consists of electron and hole currents. Electrons are ***injected*** into the base, ***diffuse*** through the base and *eventually* ***collected*** by the collector (Fig. 3c).

(2) The base, being *p*-type, presents a barrier to electrons and does ***not*** collect electrons.

(3) The hole ***diffusion*** current, on the other hand, originated from the ***base***, manifests itself as the base current and does *not* affect the collector.

Bipolar Transistor

- The ***ratio*** of the collector current I_C to the base current I_B is, thus, the ***electron*** to ***hole diffusion components*** of the base-emitter junction.
-However, if the injection ratio of electrons to holes is ***large***, such as the case of an $n+$ -p emitter-base junction by virtue of the difference in doping level, a ***current gain*** $I_C / I_B > 1$ is realized.

- The static characteristics can be readily derived from the p-n junction theory, with proper boundary conditions.

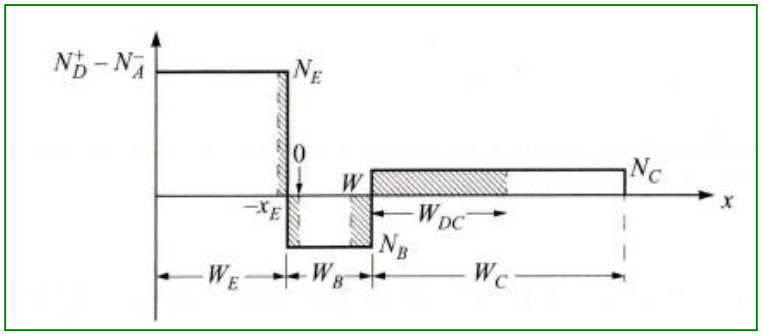
- To illustrate the *fundamental* properties of a transistor, we assume that the current-voltage relationship of the emitter and collector junctions is given by the ***ideal diode equation***, that is, the effects due to surface recombination-generation, series resistance, and high-level injection are neglected. Some of these effects will be considered later.
-We present the analysis in the *two* most-important modes-***active*** and ***saturation***, where the emitter-base junction is *forward* biased.

Bipolar Transistor

- The boundary conditions at the two edges of the neutral base region are related to the junction biases:

$$n_p(0) = n_{po}\exp\left(\frac{qV_{BE}}{kT}\right), \quad (5)$$

$$n_p(W) = n_{po}\exp\left(\frac{qV_{BC}}{kT}\right). \quad (6)$$



- With these boundary conditions, the electron distribution is known, as well as its diffusion current. The electron currents at the emitter edge I_{nE} and the collector edge I_{nC} are given by

$$I_{nE} = A_E qD_n \left.\frac{dn_p}{dx}\right|_{x=0} = \frac{A_E qD_n n_{po}}{L_n}\coth\left(\frac{W}{L_n}\right)\left\{\left[\exp\left(\frac{qV_{BE}}{kT}\right)-1\right]-\operatorname{sech}\left(\frac{W}{L_n}\right)\left[\exp\left(\frac{qV_{BC}}{kT}\right)-1\right]\right\}, \quad (7)$$

$$I_{nC} = A_E qD_n \left.\frac{dn_p}{dx}\right|_{x=W} = \frac{A_E qD_n n_{po}}{L_n}\operatorname{cosech}\left(\frac{W}{L_n}\right)\left\{\left[\exp\left(\frac{qV_{BE}}{kT}\right)-1\right]-\coth\left(\frac{W}{L_n}\right)\left[\exp\left(\frac{qV_{BC}}{kT}\right)-1\right]\right\} \quad (8)$$

where A_E is the cross-sectional area of the emitter-base junction.

- These electron currents are valid for both the ***normal*** mode and ***saturation*** mode.

Bipolar Transistor

- In the normal mode, $V_{BC} < 0$, and $n_p(W) = 0$, the electron currents at the two boundaries are given by

$$I_{nE} = \frac{A_E q D_n n_{po}}{L_n} \coth\left(\frac{W}{L_n}\right) \exp\left(\frac{qV_{BE}}{kT}\right), \quad (9)$$

$$I_{nC} = \frac{A_E q D_n n_{po}}{L_n} \operatorname{cosech}\left(\frac{W}{L_n}\right) \exp\left(\frac{qV_{BE}}{kT}\right). \quad (10)$$

- The ratio of I_{nC} / I_{nE} is called the ***base transport factor*** α_T, The difference of I_{nE} and I_{nC} contributes to part of the base current. It can be seen that for $W \ll L_n$, I_{nE} is very close to I_{nC}. In the limit of small W,

$$I_{nE} \approx I_{nC} \approx \frac{A_E q D_n n_{po}}{W} \exp\left(\frac{qV_{BE}}{kT}\right) \approx \frac{A_E q D_n n_i^2}{W N_B} \exp\left(\frac{qV_{BE}}{kT}\right) \quad (11)$$

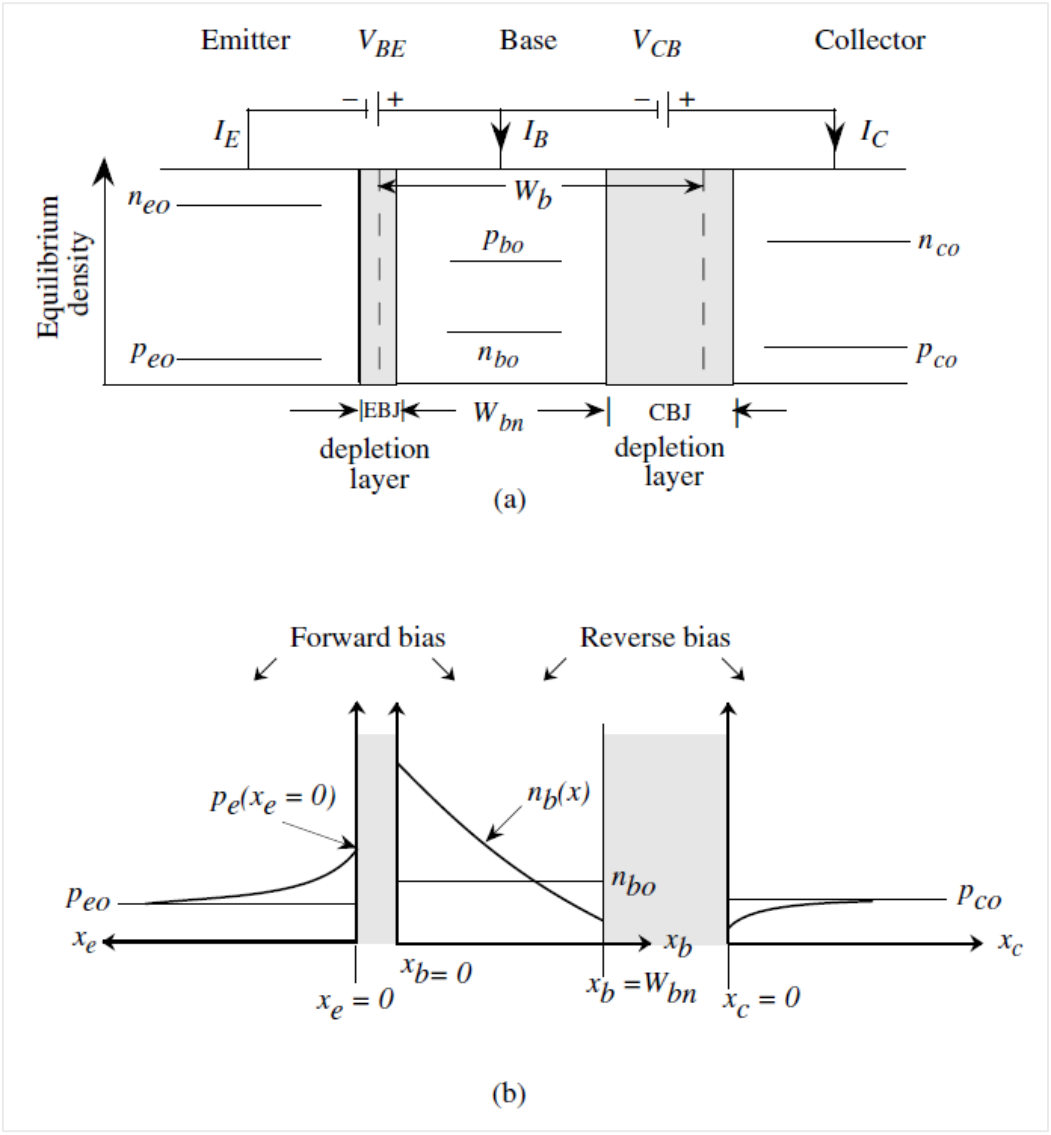
and $\alpha_T \approx 1$. Equation (11) can be reduced to a simpler form

$$I_{nE} \approx I_{nC} \approx \frac{2A_E D_n Q_B}{W^2} \quad (12)$$

where Q_B is the injected excess charge in the base,

$$Q_B = q\int_0^W [n_p(x) - n_{po}]dx \approx \frac{qWn_{po}}{2} \exp\left(\frac{qV_{BE}}{kT}\right) . \quad (13)$$

Bipolar Transistor



- A forward active mode BJT.

(a) The equilibrium carrier concentrations of electrons and holes and positions of the junction depletion regions in the npn transistor.

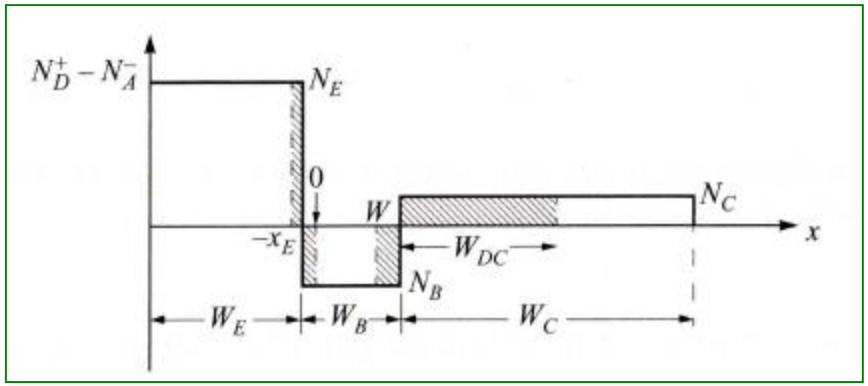
(b) Minority carrier distributions in the emitter, base, and collector regions

from "Semiconductor Device Physics and Design" by U. Mishra and J. Singh (Springer, 2008)

Bipolar Transistor

-On the other ***extreme***, if $W \rightarrow \infty$ or $W/L_n \gg$ I, the electron current at the collector I_{nC} is zero and there is no communication between the emitter and the collector. The transistor action is thus lost.

- To *improve* the base transport factor, the *uniform doping* in the base layer is usually replaced by a distribution as shown in Fig. 4.



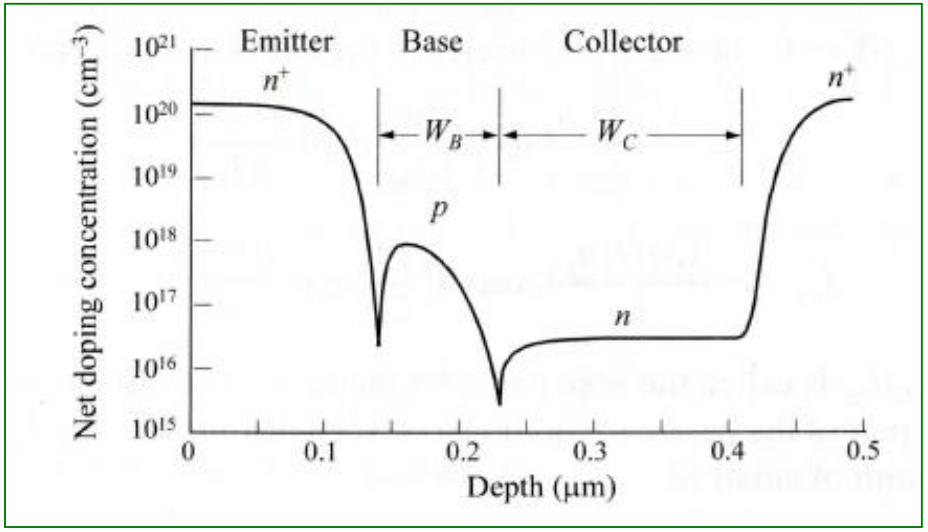
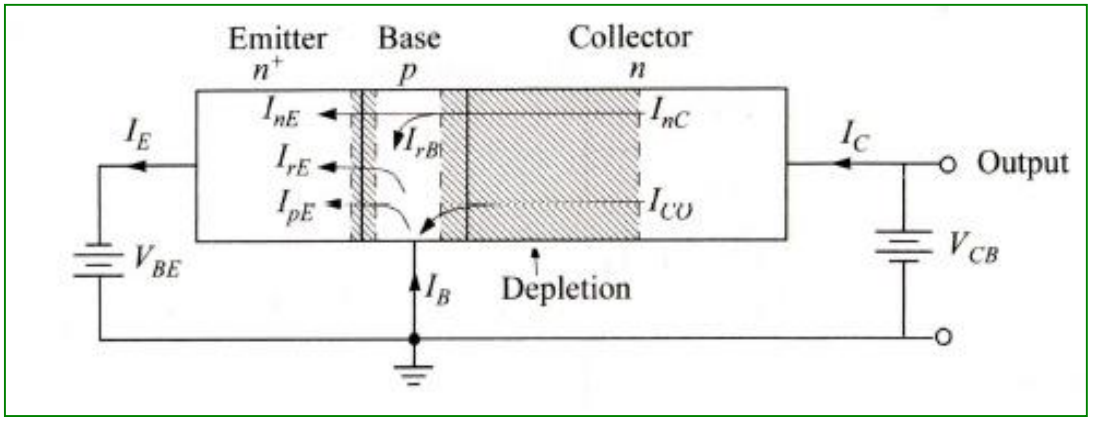


Fig. 4 Typical doping profile of a Si bipolar transistor, with an impurity gradient in the base, and a heavily doped region under the collector.

Bipolar Transistor

Current Gain

- Having analyzed each current component, the terminal currents can now be summed with the aid of Fig. 3:



$$I_E = I_{nE} + I_{rE} + I_{pE}, \tag{26}$$

$$I_C = I_{nC} + I_{CO}, \tag{27}$$

$$I_B = I_{pE} + I_{rE} + (I_{nE} - I_{nC}) - I_{CO}. \tag{28}$$

- From Kirchhoff's law and directions of the currents, it holds true that

$$I_E = I_C + I_B. \tag{29}$$

Bipolar Transistor

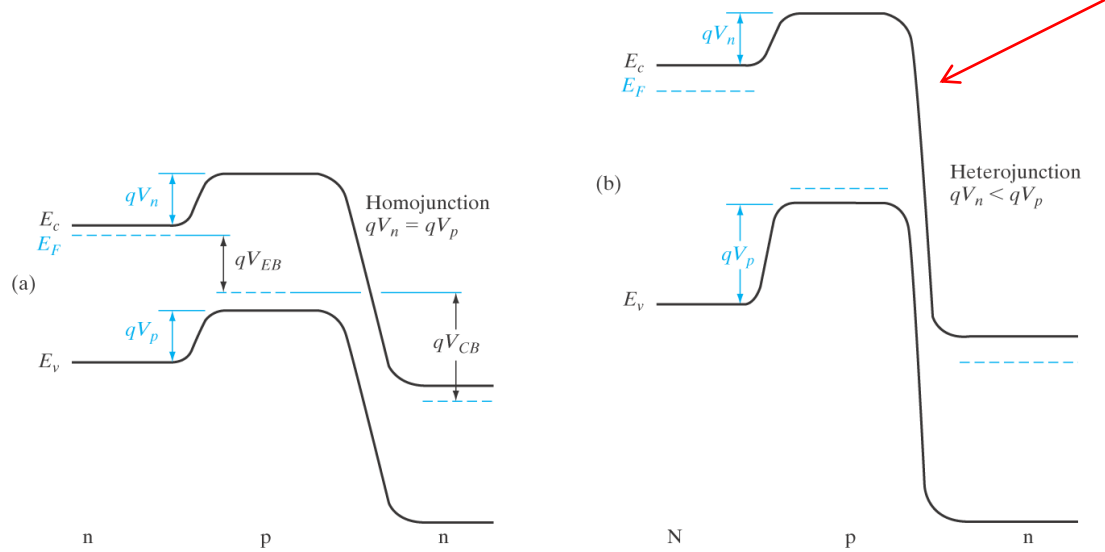


Figure 7.26

Contrast of carrier injection at the emitter of (a) a homojunction BJT and (b) a heterojunction bipolar transistor (HBT). In the forward-biased homojunction emitter, the electron barrier qV_n and the hole barrier qV_p are the same. In the HBT with a wide band gap emitter, the electron barrier is smaller than the hole barrier, resulting in the preferential injection of electrons across the emitter junction.

Heterojunction bipolar transistor (HBT).

It is possible in such a structure for the barrier for electron injection (qV_n) to be smaller than the hole barrier (qV_p). The ratio of electron current to hole current crossing the emitter junction is proportional to the ratio of the doping. In the HBT there is an additional factor in which the band gap base appears in an exponential factor.

$$\frac{J_n}{J_p} = \frac{N_{D1}}{N_{A2}} \exp\left(\frac{-\Delta E_g}{kT}\right)$$

Bipolar Transistor

-Figure 5 shows typical base and collector characteristics in the normal mode, as a function of base-emitter voltage V_{BE} .

- It can be seen here that the current gain ≈ I_C / I_E is large, and it is quite constant in most of the current range.

- Conventional parameters for a bipolar transistor are listed in Table 2.

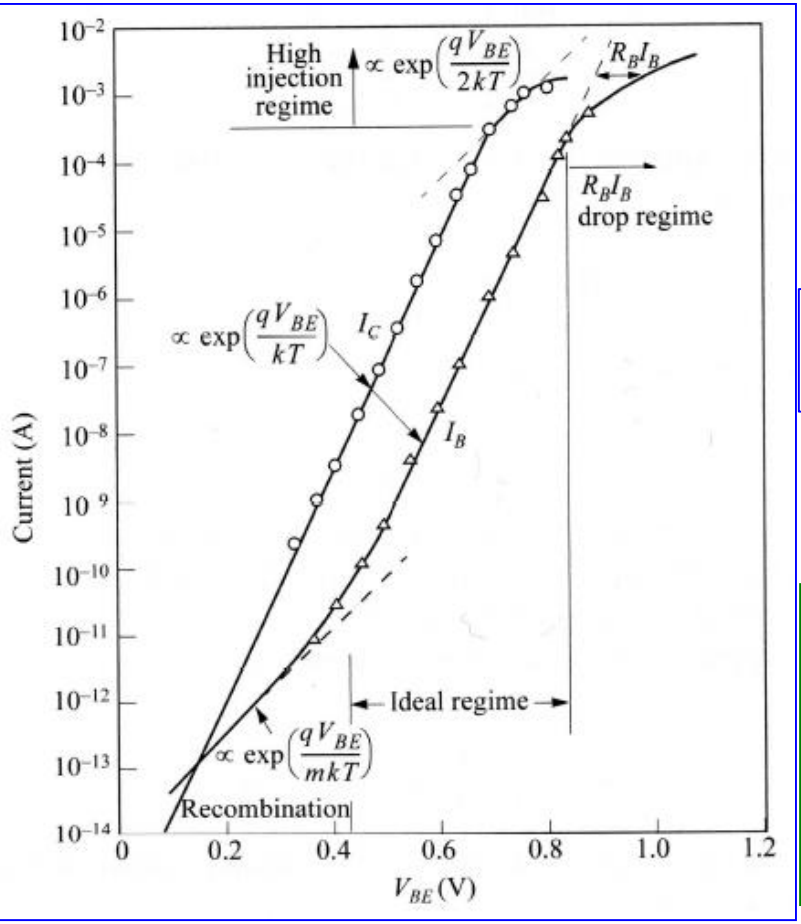


Fig. 5 Collector and base currents as a function of base-emitter voltage.

Table 2 Conventional Parameters for a Bipolar transistor

Emitter injection efficiency	$\gamma \equiv I_{nE}/I_E$
Base transport factor	$\alpha_T \equiv I_{nC}/I_{nE}$
Common-base current gain, h_{FB}	$\alpha_0 \equiv I_{nC}/I_E = \gamma\alpha_T \approx I_C/I_E$
„ small signal h_{fb}	$\alpha \equiv dI_C/dI_E$
Common-emitter current gain, h_{FE}	$\beta_0 \equiv \alpha_0/(1-\alpha_0) \approx I_C/I_B$
„ small signal h_{fe}	$\beta \equiv dI_C/dI_B$

MOSFETs

6.1 INTRODUCTION

- The metal-oxide-semiconductor field-effect transistor (**MOSFET**) is the most-important device for forefront high-density integrated circuits such as microprocessors and semiconductor memories. It is also becoming an important power device.

- The principle of the surface field-effect transistor was ***first*** proposed in the early 1930s by Lilienfeld and Heil.

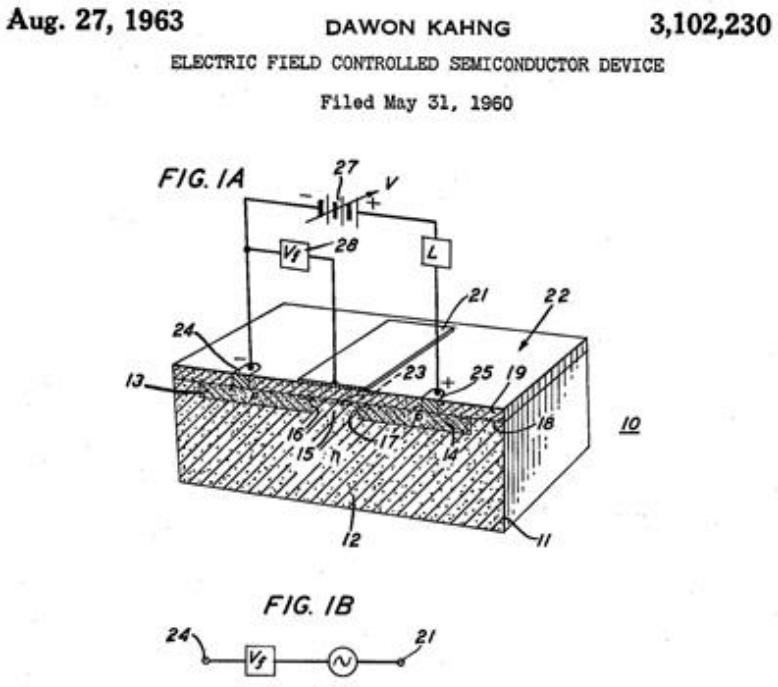
- It was subsequently studied by Shockley and Pearson in the late 1940s.

- In 1960, Ligenza and Spitzer produced the first device-quality Si-SiO_2 MOS system using thermal oxidation .

-The basic MOSFET structure using this Si-SiO_2 MOS system was proposed by Atalla. Subsequently the first MOSFET was reported by **Kahng** and Atalla in 1960.

-The basic device characteristics have been ***initially*** studied by Ihantola and Moll, Sah, and Hofstein and Heiman.

The First MOSFET at Bell Lab (1959)



Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

Filed May 31, 1960

FIG. IA

FIG. IB

US patent for the first MOSFET

Dawon Kahng (S'56–M'60–F'72) was born on May 4, 1931 in Seoul, Korea. After serving with the Korean Marine Corps, he resumed his studies at Seoul University, Seoul, Korea, and in 1955, received the B.Sc. degree in physics. He received the M.Sc. and Ph.D. degrees from Ohio State University, Columbus, OH, in 1956 and 1959, respectively.

While at Ohio State University, he was engaged in teaching as well as in the study of diffusion of impurities into silicon through a growing oxide layer. He joined Bell Laboratories, Murray Hill in 1959 and worked on feasibility studies of MOS transistors and hot electron devices on silicon epitaxial film doping profile studies. Since 1964, he has been supervising groups concerned with the development of Schottky barrier high-frequency diodes, studies of large gap and ferroelectric semiconductors, and luminescence in the visible and charge-coupled devices. More recently, he has been concerned with development of nonvolatile semiconductor memories and associated silicon integrated circuits.

Dr. Kahng is a member of Sigma Xi and Pi Mu Epsilon. He is a Life Member of the Korean Physical Society. He has authored or coauthored more than thirty-five technical articles, including a book chapter, and holds twenty-two U.S. Patents. He is a recipient of the 1975 Stuart Ballantine Medal of the Franklin Institute.

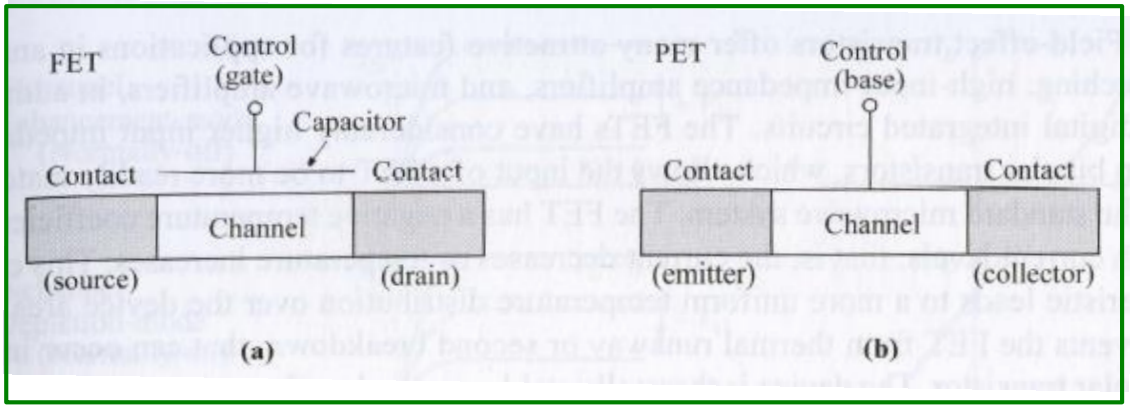
Co-inventor of MOSFET
Dawon Kahng, 강 대원 (1959)

FETs : Family Tree

- The MOSFET is the main member of the family of field-effect transistors.
- A distinction between the field-effect transistor (**FET**) and the potential-effect transistor (**PET**) is warranted here. A transistor in general is a three-terminal device where the channel resistance between two of the contacts is controlled by the third (MOSFETs have the fourth terminal as contact to the substrate).
-The difference between the FET and the PET is the way that the control is coupled to the channel.

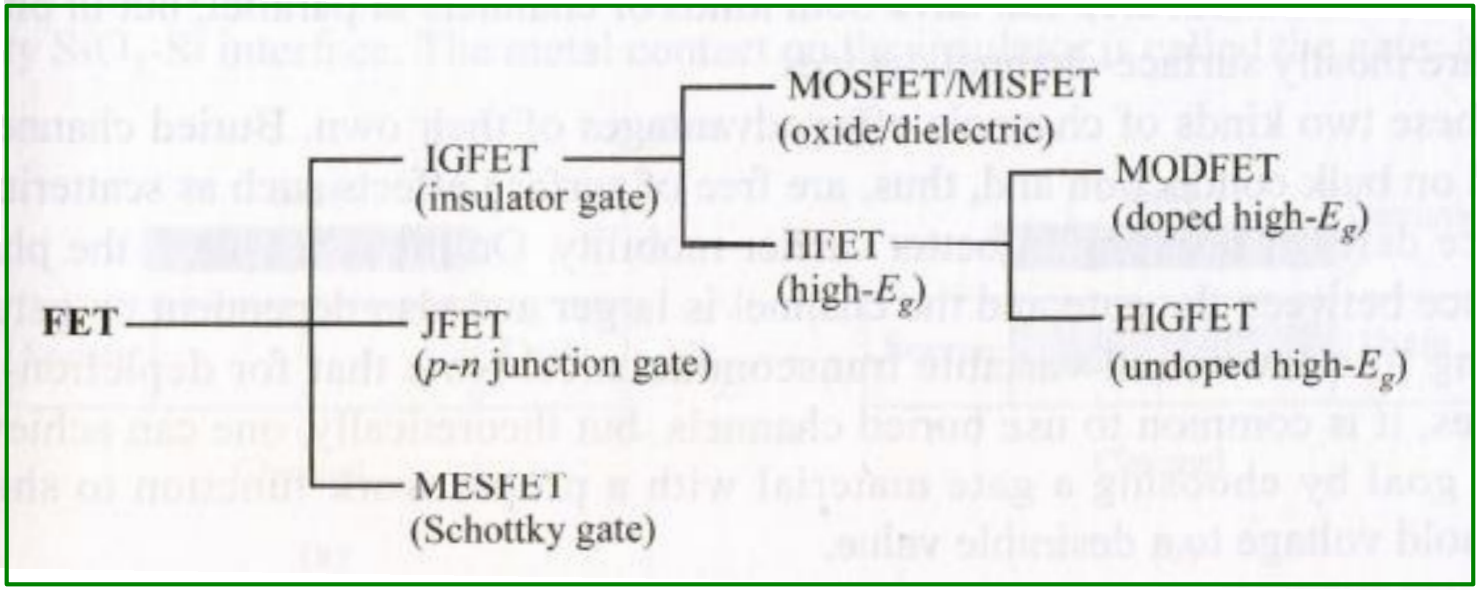
- As shown in the figure, in an **FET**, the channel is controlled ***capacitively*** by an electric field (hence the name field effect), and in a **PET**, the channel's potential is accessed ***directly*** (hence the name ***potential-effect***).

- Conventionally in FETs, the channel carriers flow from the source to the drain, and the ***control*** terminal is called the ***gate***, whereas in PETs, these corresponding terminals are called the emitter, collector, and ***base***, respectIvely.
- The ***bipolar transistor*** is a good representative of the PETs.



FETs : Family Tree

- A family tree of field-effect transistors is shown below.

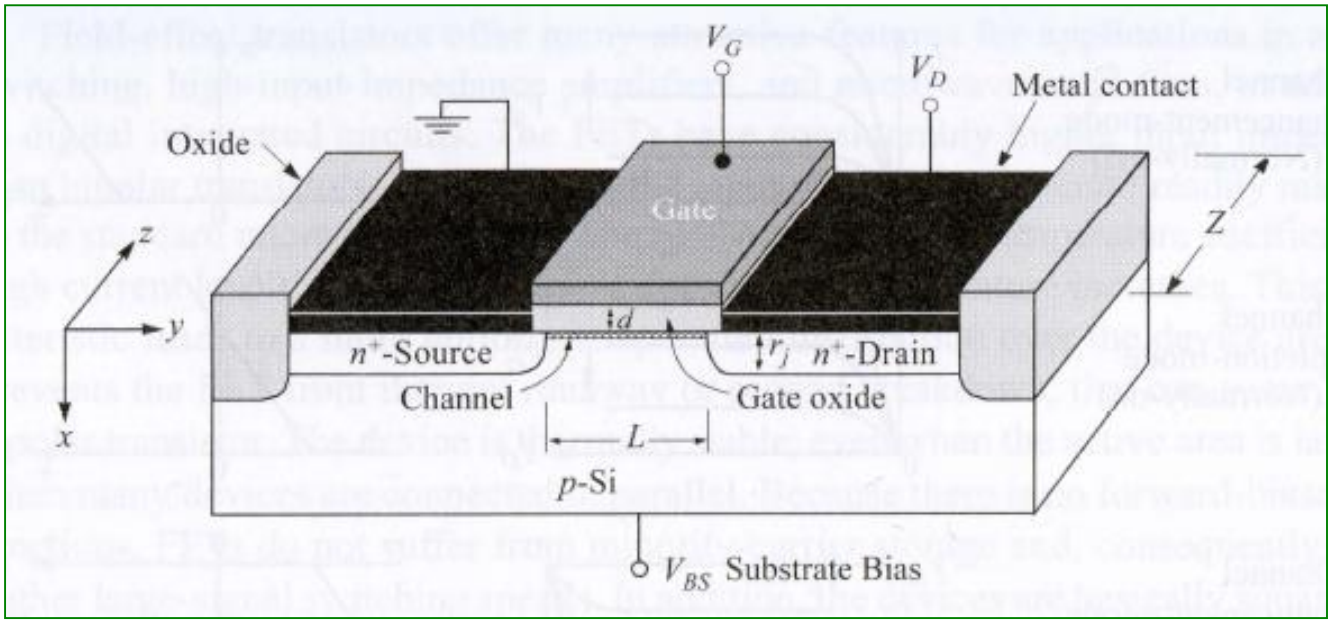


Basic Device Characteristics

- The basic structure of a MOSFET is illustrated below.

- We *assume* the channel carriers are **electrons** – an *n*-channel device. All discussion and equations will be applicable to the counterpart *p*-channel devices with appropriate substitution of parameters and the reversal of polarity of the applied voltages.

- A *common* MOSFET is a ***four***-terminal device that consists of a *p*-type semiconductor substrate into which two n^+-regions, the source and drain, are formed, usually by ion implantation.



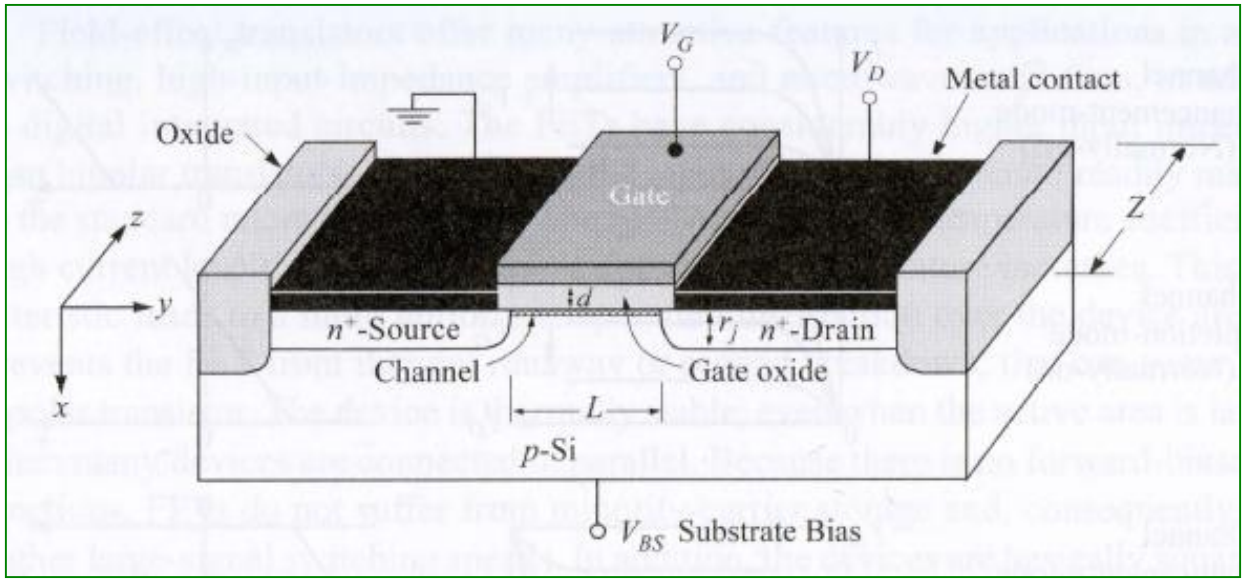
Basic Device Characteristics

-The SiO_2 gate dielectric is formed by thermal oxidation of Si for a high quality SiO_2-Si interface.

- The metal contact on the insulator is called the **gate**; heavily doped polysilicon or a combination of silicide and polysilicon is more commonly used as the gate electrode.

- The basic device parameters are the *channel length* ***L*** , which is the distance between the two metallurgical n^+-p junctions; the channel width ***Z***; the insulator thickness ***d***; the junction depth r_j ; and the substrate doping N_A.

-In a silicon integrated circuit, a MOSFET is surrounded by a thick oxide (called the field oxide to distinguish it from the gate oxide) or a trench filled with insulator *to electrically isolate* it from adjacent devices.



Basic Device Characteristics

- The source contact will be used as the voltage reference throughout this chapter.
-When ground or a ***low*** voltage is applied to the gate, the main channel is shut off, and the source-to-drain electrodes correspond to two *p*-*n* junctions connected back to back.

- When a sufficiently ***large*** positive bias is applied to the gate so that a ***surface inversion layer*** (or channel) is formed between the two n^+-regions, the source and the drain are then connected by a conducting **surface *n*-channel** through which a large current can flow.

- The conductance of this channel can be **modulated** by varying the **gate voltage**.

-The back-surface contact (or substrate contact) can be at the reference voltage or ***reverse*** biased; this substrate voltage will also affect the channel conductance.

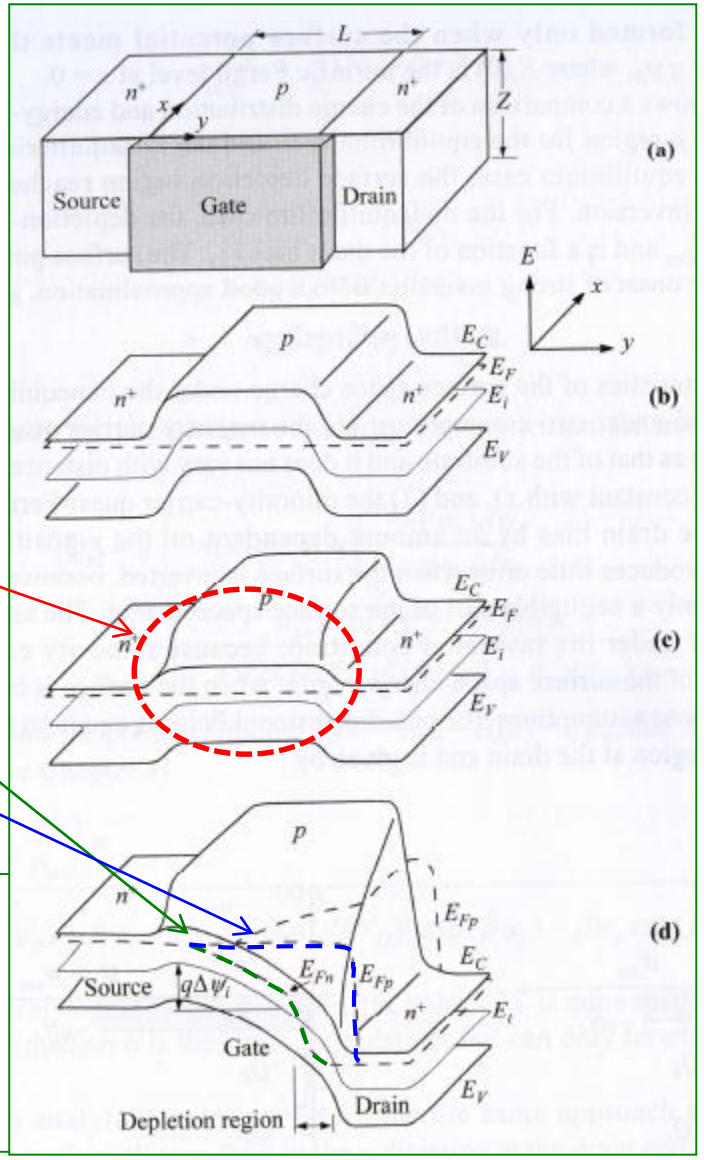
-When a voltage is applied across the source-drain contacts, the MOS structure is in a ***nonequilibrium*** condition; that is, the ***minority***-carrier (electron in the present case) quasi-Fermi level E_{Fn} is lowered from the equilibrium Fermi level.

Basic Device Characteristics

- The two-dimensional, flat-band, zero-bias ($V_G = V_D = V_{BS} = 0$) ***equilibrium*** condition is shown in Fig. 7b.

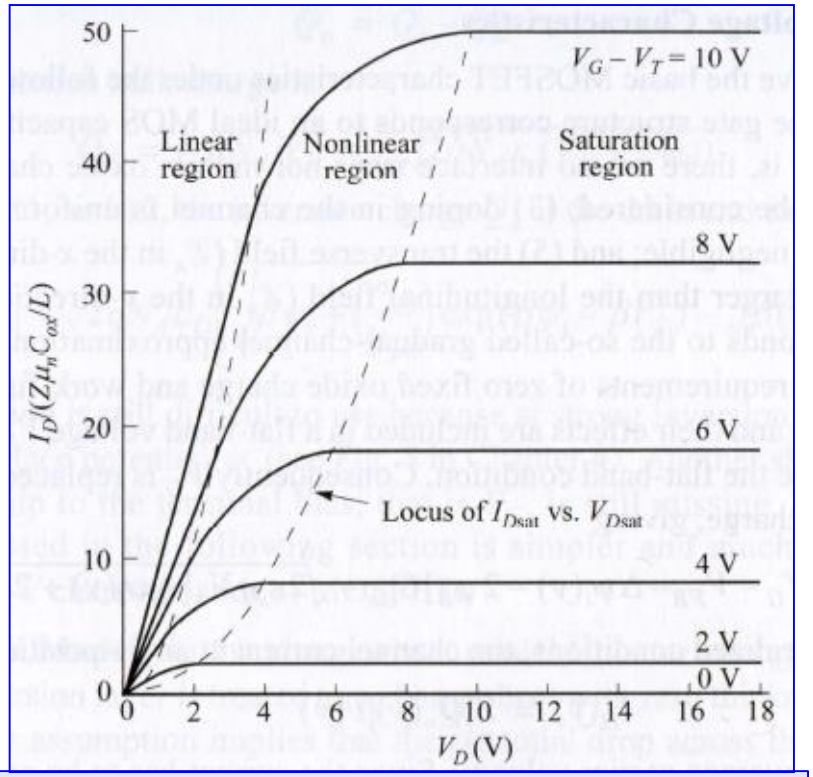
- The ***equilibrium*** condition but under a gate bias that causes surface inversion is shown in Fig. 7c.

- The ***nonequilibrium*** condition with both drain and gate biases is shown in Fig. 7d, where we note the separation of the quasi-Fermi levels of electrons E_{Fn} and holes E_{Fp} ; the E_{Fp} remains at the bulk Fermi level while E_{Fn} is lowered toward the drain contact.

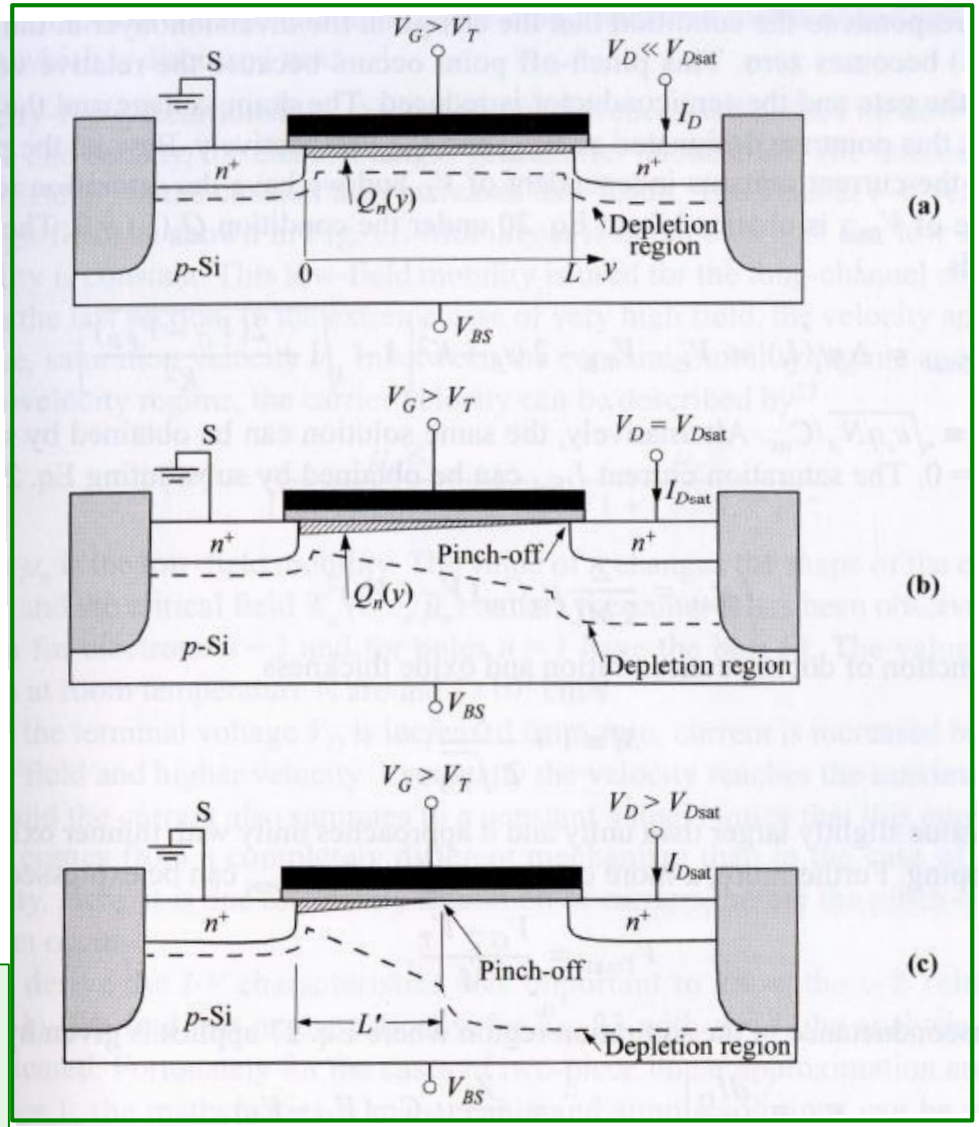


Two-dimensional band diagram of an n-channel MOSFET.
(a) Device configuration.
(b) Flat-band zero-bias equilibrium condition.
(c) Equilibrium condition ($V_D = 0$) under a positive gate bias.
(d) Nonequilibrium condition under both gate and drain biases.

Basic Device Characteristics



Idealized drain characteristics (I_D vs. V_D) of a MOSFET. The dashed lines separate the linear, nonlinear, and saturation regions.



MOSFET operated (a) in the linear region (low V_D), (b) at onset of saturation, and (c) beyond saturation