Fabrication and Characteristics of High-Speed Implant-Confined Index-Guided Lateral-Current 850-nm Vertical Cavity Surface-Emitting Lasers

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***Abstract*—Process technology of high-speed implant-apertured index-guide lateral-current-injection top dielectric-mirror quantum-well 850-nm vertical cavity surface-emitting lasers (VCSELs) has been developed. Oxygen and helium implantation for aperture definition and extrinsic capacitance reduction, dielectric mirror formation, p- and n-ohmic contact formation, VCSEL resistance, and thermal analysis were investigated. Employing this technology, GaAs/AlGaAs-based 850-nm VCSELs with small signal modulation bandwidths up to 11.5 Gb/s and an eye diagram generated at 12 Gb/s by a pseudorandom bit sequence of $2^{31}-1$ were achieved. The bit-error rates were below 10^{-13}. The threshold current is as low as 0.8 mA for 7-μm-diameter current apertures and typical slope efficiencies of 0.45–0.5 mA/mW were obtained.**

***Index Terms*— 850-nm vertical cavity surface-emitting laser (VCSEL), lateral current injection, vertical cavity surface-emitting laser (VCSEL) process integration.**

I. Introduction

TREMENDOUS progress has been achieved in development of vertical cavity surface-emitting lasers (VCSELs) for high-speed optical interconnects in high-bit-rate data transmission systems [1]–[12]. Most of the devices are based on an oxide-confined structure, which has proven to provide low thresholds, good thermal resistance, and good optical confinement. The oxide-aperture VCSEL design contains only one heterointerface for current to pass through, lowering the p-contact resistance and reducing the lasing threshold voltage. The oxide also serves to electrically isolate the devices from each other. In this design, the oxide formed acts as an index guide having a different refractive index from that of the active layer. This serves to create laser emission with greater model coherence.

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Although the selectively oxidized VCSELs have excellent device performance, there are still issues of control of oxidation rate and therefore of device reproducibility in situations requiring high process yields. The lateral oxidation rate depends on material and processing parameters, introducing variations into the final aperture size. For example, to illustrate the sensitivity of $Al_xGa_{1-x}As$ wet-oxidation rate to material composition, orders of magnitude variation in oxidation rate was observed for $0.84 < \times < 1$ [6]. Variations in feature size will lead to difficulty in meeting stringent specifications required by envisioned VCSEL applications such as integration into CMOS circuits [12]. Apertures formed by ion implantation have produced VCSELs with comparable device dc performance to oxide-confined apertures [6]. The implant-apertured VCSEL offers the potential for a highly reproducible process, since the aperture feature is defined by photolithography. Historically, implant apertured VCSELs have had worse modal coherence than oxide-confined structures, due to the simultaneous optical and confinemental in the latter. However, the addition of an index guide formed external to the active layer of implant apertured VCSELs can improve model coherence [13].

In this paper, we report on layer structure design, ion implantation for aperture formation and extrinsic capacitance reduction, index-guided formation, n- and p-ohmic metallization, resistance and thermal simulation for lateral current injection, and index-guide implanted-aperture quantum-well VCSELs. DC, small signal, and large signal measurements were performed on GaAs quantum-well 850-nm VCSELs fabricated based on this technology.

II. Layer Structure Design and Epitaxial Growth

A schematic of the layer structure for the implanted and index-guided VCSEL is shown in Fig. 1. The structures were grown by low-pressure metalorganic chemical vapor deposition. Arsine, phosphine, trimethylgallium, trimethylindium, and trimethylaluminum were used as the precursors. Carbon tetrabromide and disilane were utilized as the p- and n-dopant precursors, respectively. The majority of the structure was grown at 760 °C except for the p-lateral current injection, etch-stop InGaP, and index-guide layers, which were grown at reduced temperature in order to enhance the carbon doping in the p-lateral current injection (LCI) layers. Perfectly smooth morphology was obtained, and there was excellent agreement between the calculated and experimental reflectivity spectrum.

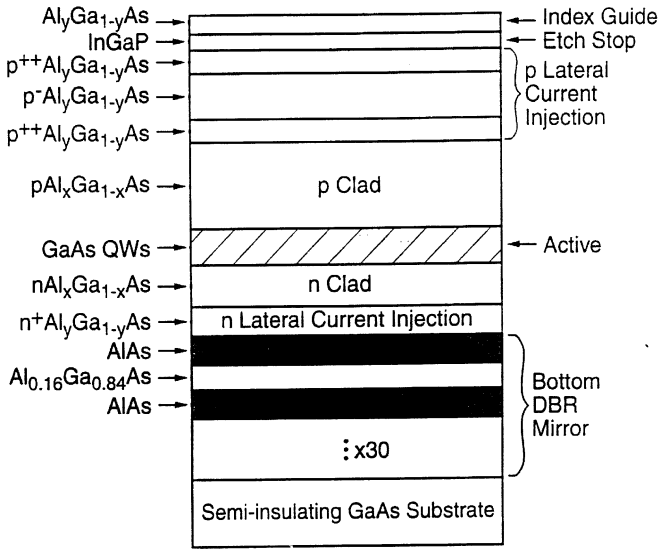

Fig. 1. Schematic of the layer structure for the implanted and index-guide VCSEL.

Secondary ion mass spectroscopy measurements confirmed the intended doping concentrations and demonstrated the low oxygen concentration in the AlGaAs layers despite the low growth temperature.

A key feature of the design is the p-lateral current injection structure. Thin (~30 nm), highly doped ($\sim 10^{20}$ cm^{-3}) $Al_yGa_{1-y}As$ (low Al content) layers are sandwiched around low doped $Al_yGa_{1-y}As$. The purpose here is to allow the current to spread uniformly across the current aperture since the central low-doped layer provides some resistance in the vertical direction. Without this type of structure, the current would flow along the periphery of the aperture, resulting in poor efficiency and preferential pumping of higher order modes. Another important point is that the p^{++} $Al_yGa_{1-y}As$ layers are placed at the nodes of the optical cavity standing wave. This greatly minimizes free carrier absorption. The InGaP layer provides an etch-stop layer for making ohmic metal contact to the top p^{++} $Al_yGa_{1-y}As$ layer. The index guide layer thickness can be chosen to control the degree of guiding desired for a given index guide diameter (see below).

The active region consists of several GaAs quantum wells with $Al_{0.2}Ga_{0.8}As$ barriers. The p-cladding $Al_xGa_{1-x}As$ $(x \sim 0.5)$ is thicker than the n-cladding layer in order to form a significantly wide implant isolation layer. The n-LCI layer consists of highly doped $Al_yGa_{1-y}As$). Because of the high conductivity of this layer, the current crowding effect is not an issue. The lower $AlAS/Al_{0.16}Ga_{0.84}As$ distributed Bragg reflector (DBR) mirror is undoped, and an undoped semi-insulating GaAs substrate is used for high-speed laser performance. The top dielectric mirror, described below, is deposited following processing of the device. One of the advantages of this structure is the use of undoped mirrors, which minimizes free carrier absorption.

III. Device Fabrication

A. Implantation

A schematic cross section of the fabricated implanted and index-guided VCSEL and process flow is shown in Figs. 2 and 3. The first two process steps are implantations. Fig. 4 shows the implant profiles of the simulated O^+ and He^+ for aperture formation and extrinsic capacitance reduction, respectively. Oxygen is typically used for the first, shallow implant to form the current aperture. The dose must be high enough to create damage sufficient to compensate the free carrier concentration of the $p - Al_xGa_{1-x}As$ cladding layer. The implant energy is also critical since damaging the active region will effect the device reliability. If the implant range is too shallow, then leakage current above the active will increase the threshold current.

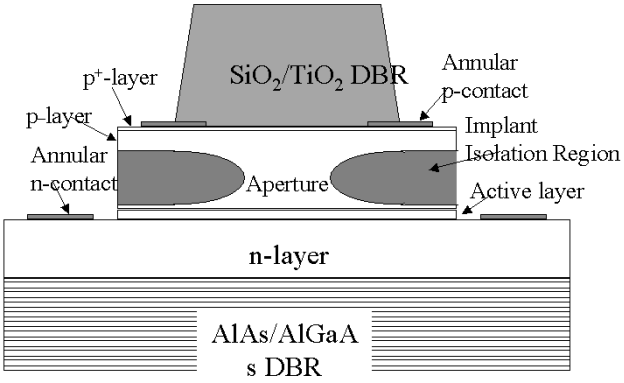

Fig. 2. Cross-sectional view of an 850-nm VCSEL.

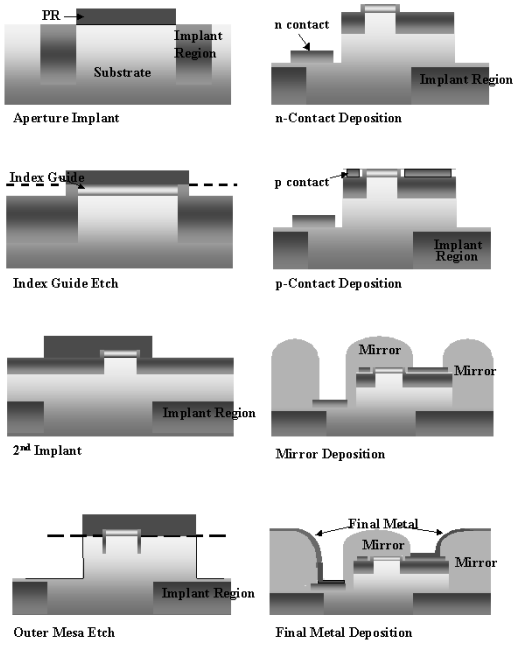

Fig. 3. Process sequence of an 850-nm VCSEL.

A second, deep implant can be used to reduce the capacitance of the laser. Typically helium can be used for this purpose. It is necessary to eliminate the n-LCI layer conductivity in areas under the p-type layers while leaving some area for current injection.

B. Index Guide and p-Mesa Formation

The next step is index guide formation. It is formed by selectively etching the top $p - Al_yGa_{1-y}As$ layer with the $In_{0.5}Ga_{0.5}P$ serving as an etch-stop layer. The thickness of the

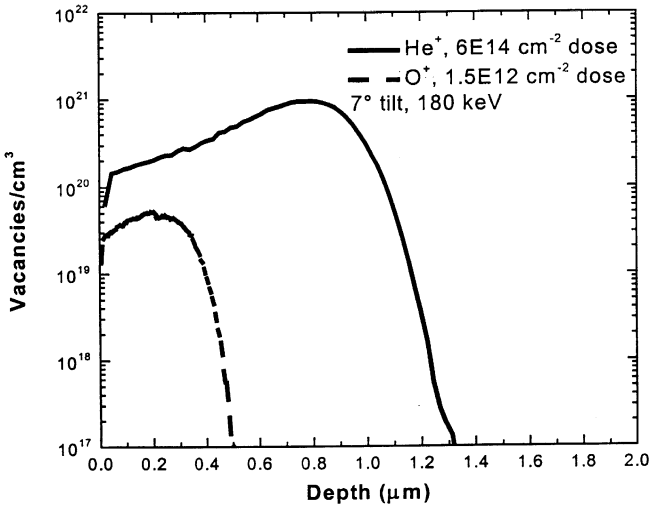

Fig. 4. Simulation O^+ and He^+ implant profiles.

index guide is accurately controlled by the epitaxial growth, and the lateral dimensions can be varied by the appropriate mask design. These two parameters control the degree of index guiding for a given aperture size. The etch selectivity of $In_{0.5}Ga_{0.5}P$ over AlaGaAs is over 200.

Following the index guide formation is p-mesa definition, which is achieved with wet chemical etching using resist as an etch mask. The etch depth of p-mesa has a significant impact on the n-contact resistance. Underetch during the p-mesa definition causes the high specific contact resistivity due to the n-metallization being formed on the low doped and high Al concentration of the n-AlGaAs cladding layer. On the other hand, overetch creates high sheet resistance of the n-LCI layer.

C. p-Ohmic Contacts

After the mesa etching of the VCSEL, the challenging part of the process is formation of low-resistance ohmic contacts to the p- and n-LCI layers [14]–[18]. Low device resistance is essential for high-speed performance in VCSELs, and forming low resistant intracavity p- and n-contacts on VCSELs is one of the prerequisites [14]–[18]. Intracavity contacts are contacts formed to semiconductor layers inside the optical cavity of the VCSEL, and can thus shorten the current transport distance through the active region of the VCSEL. Intracavity contacts have been demonstrated for very low contact resistance in high-speed shallow-implanted 980-nm VCSELs [19]. For these devices, contacts were made to highly doped GaAs layers. For the case of 850-nm VCSEL, the contacts have to be formed on AlGaAs layers and become more challenging. The $Al_xGa_{1-x}As$ materials system oxidizes faster than GaAs, and this makes the preservation of an oxide-free AlGaAs surface for the ohmic contact formation much more difficult [20]. In our design, the p^{++} highly doped ($\sim 10^{20}cm^{-3}$) $Al_yGa_{1-y}As$ ohmic contact layer is below an undoped $Al_yGa_{1-y}As$ index guide, an undoped InGaP etch stop, and a p^+ $Al_yGa_{1-y}As$ optical space layer. This optical spacing layer is to place the p^{++} $Al_yGa_{1-y}As$ ohmic contact layer at the nodes of the optical cavity standing wave to minimize free carrier absorption in the p^{++} $Al_yGa_{1-y}As$ layer.

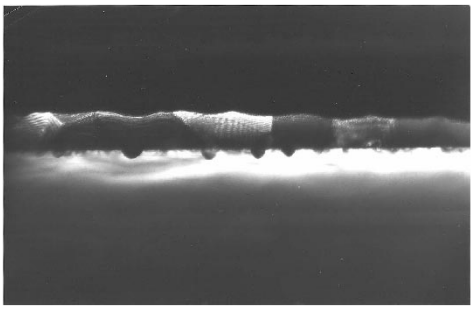

Fig. 5. TEM of annealed AuBe/Au metal contact.

To obtain the low contact resistance, all these three top layers should be etched off prior to the ohmic metal deposition. The first two layers can be easily etched off with a selective wet-etch chemical solution [21]. However, the p^+ spacing and p^{++} ohmic contact layer have the same composition. Therefore, it is impossible to etch off the p^+ $Al_yGa_{1-y}As$ spacing layer and stop right on the p^{++} $Al_yGa_{1-y}As$ ohmic contact layer reproducibly. Thus an alloyed ohmic metallization is required to diffuse through the p^+ $Al_yGa_{1-y}As$ spacing layer and form the ohmic contact to the $Al_yGa_{1-y}As$. Be is a p-dopant for GaAs, and AuBe-based metallizations can achieve this goal.

To form good p-ohmic contacts, we have to consider not only the effect of index guide, etch stop, and optical space layer on p^{++} $Al_yGa_{1-y}As$ but also the layer beneath it. A key feature in the lateral current injection VCSEL design is the use of low doped p $Al_yGa_{1-y}As$ layers to sandwich another thin highly doped p^{++} $Al_yGa_{1-y}As$ layer for current spreading. This current spreading layer is directly under the p^+ $Al_yGa_{1-y}As$ ohmic metal contact layer. The purpose here is to allow the current to spread uniformly across the current aperture since the central low-doped layer provides some electrical resistance in the vertical direction. Without this type of structure, the current would flow along the periphery of the aperture, resulting in poor efficiency and preferential pumping of higher order modes. Since this current spreading layer is right under the p^+ $Al_yGa_{1-y}As$ ohmic contact layer, it is very important to control the diffusion depth of AuBe to stop in the p^{++} $Al_yGa_{1-y}As$ layer and not penetrate into the $p-Al_yGa_{1-y}As$ current spreading layer. This is achieved by optimizing the ohmic metallization, ohmic contact annealing temperature, and annealing time.

Different combinations of AuBe [22], Au, Pt [23], Ag, Ti, and Pd [24], [25] were used in our studies. AuBe was used for the ohmic formation. Be served as the p-dopant and is diffused into AlGaAs through annealing. Au was utilized as the top contact layer to reduce the metal resistance. Pt and Ag were employed as the diffusion barrier. Without this Pt or Ag layer, the top Au contact layer can form deep Au spikes (around 300–400 nm) into the semiconductor and behave as Schottky contacts [26], [27]. Auger depth profiles of as-deposited and annealed Ti–Pt–Au and AuBe–Ag–Au samples (annealed at 400 °C for 30 s) showed no metal intermixing when Pt was used as the diffusion barrier. There was interaction among Au–Ag–AuBe at high temperature (>380 °C), and Fig. 5 shows the TEM of annealed AuBe/Au metal contact. In this case, there was no diffusion barrier employed, and deep Au spikes were clearly observed. Pd is typically used as a wet

TABLE I
SPECIFIC CONTACT RESISTANCE OF DIFFERENT METALLIZATION ON p-AlGaAs

Composition		350°C	400°C	450°C
AuBe/Ag/Au/Ti *	No implant	Schottky	10.8	8.0
	Implant	Schottky	7.4	14.7
AuBe/Pt/Au/Ti *	No implant	Schottky	50.3	13.4
	Implant	Schottky	55.8	22.2
Pd/Ti/Pt/Au *	No implant	Schottky	33.2	9.9
	Implant	Schottky	112	10.7
AuBe/Au/Ti *	No implant	87.4	5.2	6.5
	Implant	Schottky	7.5	13.5
Pd/AuBe/Pt/Au/Ti *	No implant	10.2	4.2	5.6
	Implant	580	6.1	4.1
AuBe/Au/Ti #	No implant	46	4.4	5.0
	Implant	Schottky	9.7	4.4

The specific contact resistance is in the scale of 10^{-6} Ω-cm^2.
*: Contacts were on top of p-AlGaAs.
#: Contacts were on top of InGaP.

agent to dissolve native oxides on the semiconductor surface. Ti was used for adhesion in Ti–Pt–Au metallization.

The as-deposited contacts of all the metallizations behaved as Schottky characteristics, and some of them showed ohmic nature after annealing at ~300–350 °C. Once the annealing temperature was raised to 400 °C, the specific contact resistances greatly improved to $\sim 10^{-5} - 10^{-6}\ \Omega - \text{cm}^2$, as shown in Fig. 6. For annealing temperature reaching 450 °C, the specific contact resistivity slightly reduced further, as shown in Table I. In general, the contact resistances are higher for the implanted samples due to the ion bombardment damage introduced to the p^{++}-contact layer during the aperture definition implantation. Table I also contains the information of the effects of Pd and contacts directly deposited on InGaP instead of AlGaAs on the specific contact resistivity. As mentioned previously, Pd is used as the wet agent to dissolve native oxides on the semiconductor surface and allows AuBe to diffuse into the p^{++} $Al_yGa_{1-y}As$ forming low resistant contacts. The as-deposited and annealed at 350 °C samples show ohmic characteristics. The metallization consisting of Pd and AuBe as the first two layers shows the lowest specific contact resistivity. The samples with contact metal deposited directly on the InGaP also show lower resistance as compared to that on p-AlGaAs. Native oxides on semiconductor surface hinder the ohmic formation between the contact metal and semiconductor. Since InGaP is more resistant to oxidation than AlGaAs, the lower contact resistance should be expected with the samples having metal directly on the InGaP layer.

The effect of AuBe thickness on specific contact resistivity was also studied and is shown in Fig. 7. The optimal thickness of the AuBe is around 200–300 Å; 100 Å AuBe was not enough to penetrate the p^+ $Al_yGa_{1-y}As$ optical space layer to the p^{++} $Al_yGa_{1-y}As$ layer. A value of 800 Å AuBe was too much, and AuBe reached the low-doped $p - Al_yGa_{1-y}As$ layer current spreading layer and destroyed the current spreading after annealing.

D. n-Ohmic Contact

Ge/Pd-based metallizations were studied for ohmic contacts to n-LCI $Al_XGa_{1-X}As$ layers. Annealing conditions play a role

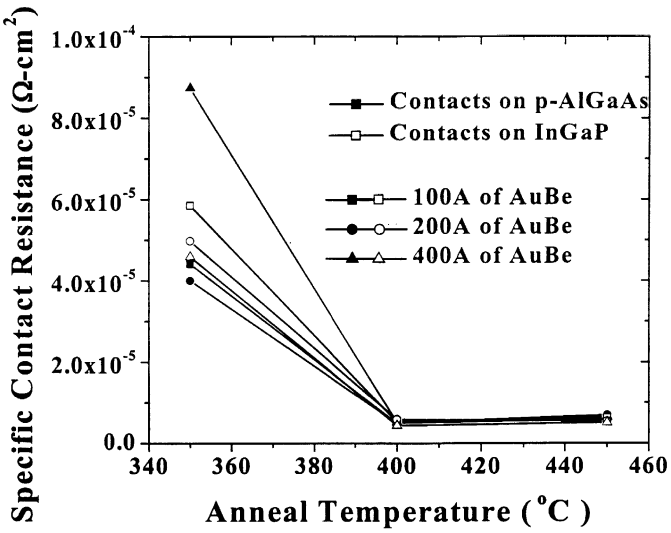

Fig. 6. Specific contact resistance of contact with varied AuBe thickness as a function of anneal temperature.

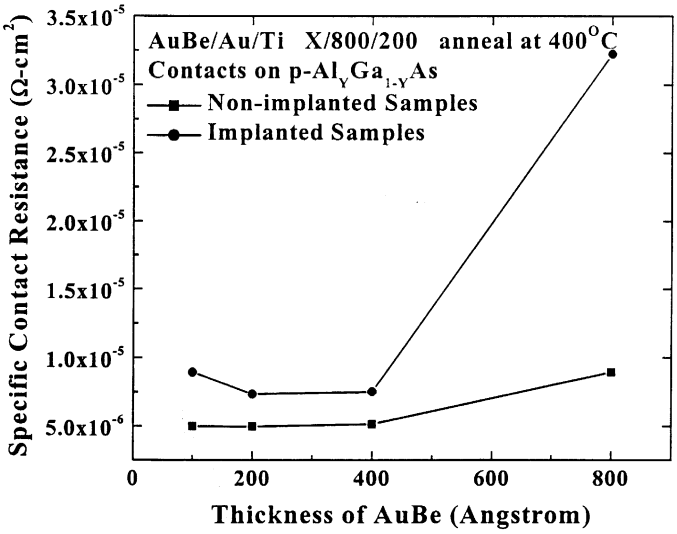

Fig. 7. Specific contact resistance of contact with and without oxygen implantation as a function of AuBe thickness.

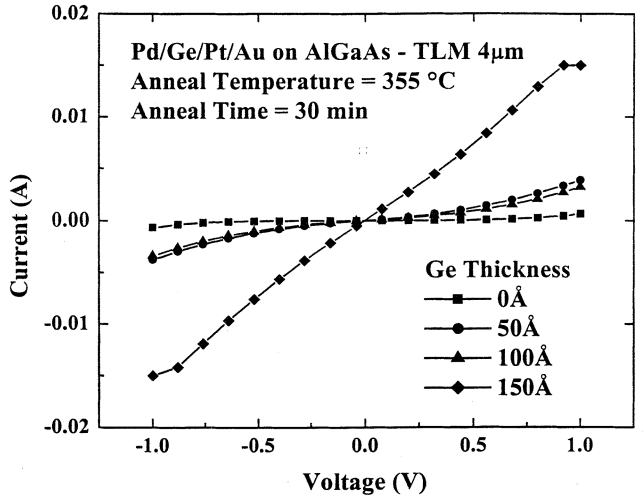

Fig. 8. Current–voltage characteristics for different Ge thickness.

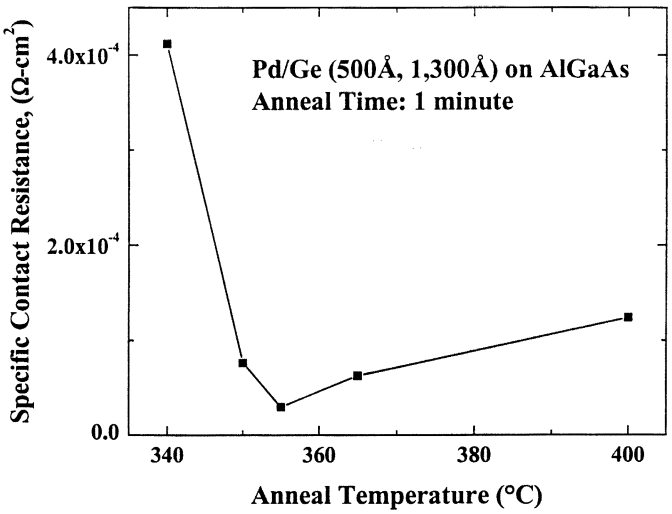

Fig. 9. Specific contact resistance as a function of anneal temperature.

in the behavior of both ohmic contacts. It has been found that Pd and Ge diffused during the annealing process of the Pd/Ge/Au contact. Good ohmic contacts were found to occur when Ge was detected at the semiconductor surface. Degradation in the ohmic contact behavior correlated with Ge further diffusion into the semiconductor beneath the contact. The layer structure of n-type lateral current injection-based VCSEL design also consists of many thin low-doped current spreading and highly doped contact layers; thus, the Ge diffusion depth has to be even more precisely controlled.

Fig. 8 shows current–voltage characteristics for different Ge thickness in Pd(100 Å)/Ge(0–500 Å)/Pt(300 Å)/Au(1200 Å) metal scheme across a 4-μm gap in the transmission line method (TLM) testing pads. The purpose of using Ge is to increase the n-type doping concentration in the AlGaAs beneath the metal contacts, which can convert a rectifying contact into an ohmic contact via the formation of a highly doped region to enhance the tunneling current. Fig. 9 shows the specific contact resistance as a function of annealing temperature. All the samples annealed in temperature range from 340 to 400°C display an ohmic behavior, and the best ohmic contact occurs at 355°C.

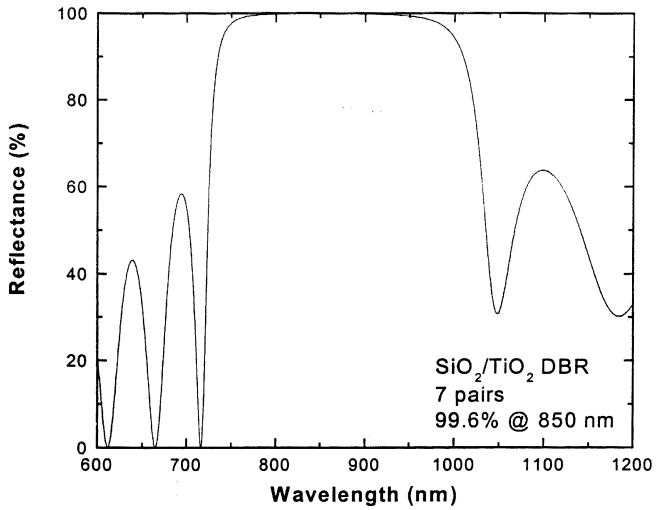

Fig. 10. Simulation reflectivity of seven pairs of SiO_2/TiO_2 mirror stack.

E. Dielectric DBR Mirror Formation

The final part of the processing is the dielectric DBR mirror formation. Mirrors fabricated with liftoff and dry and wet chemical dielectric etch-back processes were investigated. A SiO_2/TiO_2-based dielectric was used in our VCSEL, and the refractive index of SiO_2 and TiO_2 is 1.46 and 2.3 at 850 nm, respectively. To achieve a reflectivity above 99.5%, seven pairs of SiO_2/TiO_2 (150 nm/120 nm) are needed, as illustrated in Fig. 10, the reflectivity simulation. The total thickness of the seven pairs' SiO_2/TiO_2 dielectric stack is around 1.89 μm. The SiO_2 and TiO_2 were deposited with electron beam evaporation.

1) Liftoff Process: In order to reduce the internal stress of the dielectric stack, the substrate temperature was held at 200 °C during the deposition. Therefore, a Futurrex negative resist was used instead of standard positive AZ resist. The resist thickness was around 4.5 μm at 3000-rpm coating speed. The profile of the exposed and developed pattern is quite sharp and straight, as illustrated in the top of Fig. 11. After dielectric deposition, the liftoff was accomplished with a resist stripper. The bottom of Fig. 11 shows a scanning electron micrograph (SEM) of a lifted-off SiO_2/TiO_2 mirror on the top of an 850-nm VCSEL. Excellent adhesion and yield of the dielectric were achieved. However, the edge of the liftoff dielectric stack was jagged, which may limit the minimization of the VCSEL aperture.

2) Dry Etch-Back Process: Cl_2/Ar and SF_6/Ar discharges were used to etch SiO_2/TiO_2 mirror samples. For the Cl_2/Ar chemistry, three runs were performed (500 W ICP, 100 W RF; 500 W ICP, 150 RF; and 500 W ICP, 250 W RF), and very low etch depths were obtained after 5-min etches. This suggests a limiting etch rate from one of the layers. Etch experiments with single layers of SiO_2 only and TiO_2 only were performed to obtain the etch rate of the individual layers. It was found that SiO_2 etches $\sim$3 times faster than TiO_2 in Cl_2/Ar at 500 W ICP/250 W RF. The etch rates of SiO_2 and TiO_2 were 800 and 280 Å/min, respectively. The etch product of TiO_2, $TiCl_x$, is not very volatile, and therefore slows down the mirror etch. To etch the entire mirror stack using this chemistry would require more than 50 min, in which time the resist mask will have been etched through.

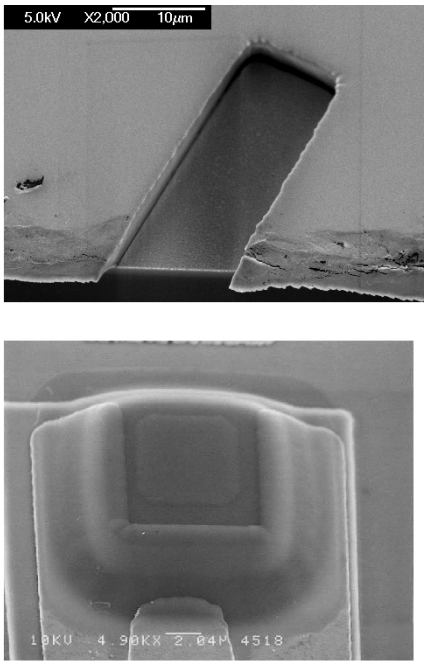

Fig. 11. (Top) The profile of exposed and developed pattern was quite sharp and straight, as illustrated in Fig. 6. (Bottom) An SEM of a liftoff SiO_2/TiO_2 mirror on top of an 850-nm VCSEL.

Fig. 12 shows the etch rates of an SiO_2/TiO_2 mirror stack in SF_6/Ar and in Cl_2/Ar discharges. The etch rates of the mirror stack in SF_6/Ar are around two to three times faster than in the Cl_2/Ar chemistry. This is due to the fact that the TiO_2 etch product TiF_4 in SF_6 is quite volatile, and the etch rates of SiO_2 and TiO_2 in SF_6/Ar are comparable. As radio-frequency (RF) power was increased, the ion energy increased. A faster etch rate was achieved with increasing RF power. As the inductively coupled plasma (ICP) power increased, the ion density increases. The etch rate was also enhanced with increasing ICP power. The highest etch rate obtained was 1200 Å/min, and using the conditions for this etch rate, the total etch time for the entire mirror was reduced to 15 min. Fig. 13 shows an SEM of a dry-etched mirror stack. Sharp edge definition was achieved using this process.

3) Wet Chemical Etch-Back Process: Wet oxide etchants HF and BOE were also used to etch the SiO_2/TiO_2 DBR mirror stacks. Good etch rates were obtained using BOE and dilute HF:H_2O (1:3). The etch rates were ∼2050 A/min and ∼2.7 μm/min, respectively. However, as shown in Fig. 14, significant etch undercut and delamination between SiO_2/TiO_2 interfaces were observed. This is due to internal stress between the layers of the dielectric DBR mirror. Some of the undercut observed extended more than 10–15 μm, which is larger than the dimensions of some of the mirror features. Therefore, the wet chemical process is not suitable for dielectric mirror patterning, as of now. A higher dielectric deposition temperature may help to anneal out the stress. Nevertheless, additional careful studies are needed. We use a commercially available TiO_2/SiO_2 multilayer mirror stack defined by a photolithographic liftoff process. The reflectivity is determined by the number of $\lambda/4$n layers. We typically choose an output reflectivity of 99.5%.

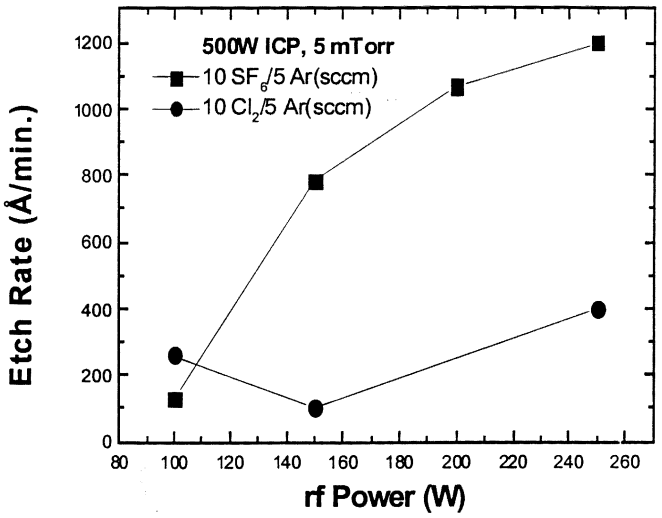

Fig. 12. Etch rates of an SiO_2/TiO_2 mirror stack in SF_6/Ar and in Cl_2/Ar discharges.

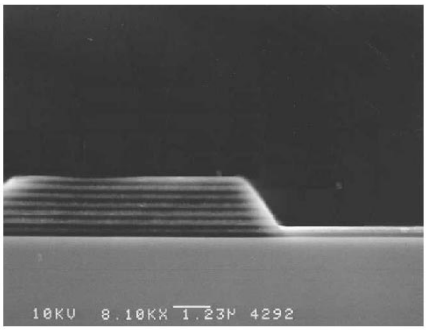

Fig. 13. SEM of a dry-etched SiO_2/TiO_2 mirror stack.

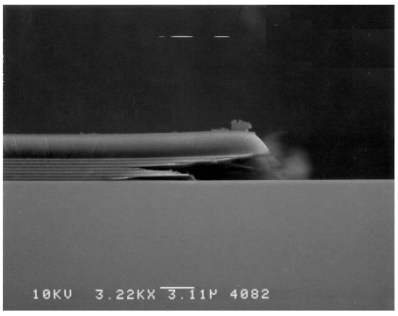

Fig. 14. SEM images of a dielectric mirror stack patterned with wet etchants (a) HF or (b) BOE. The photoresist mask can be seen in both images.

IV. Resistance Simulations

The individual resistances arising from current transport through the semiconductor layers and the ohmic contacts in an implant-apertured index-guided 850-nm VCSEL have been calculated from Hall and transmission-line method data. The results can be used to simulate the expected VCSEL current–voltage characteristic, which shows excellent agreement with the experimental data. This process provides a simple method for predicting the effect of changes in epitaxial layer structure thicknesses, doping, and materials on the dc characteristics of high-performance VCSELs.

In creating new VCSEL designs or in attempting to understand the effect of contact quality on VCSEL performance, it is useful to be able to have a simple method for predicting the impact of these changes on the dc characteristics. A key parameter in this regard is the distributed resistance for the diode. Device resistance in VCSELs has contributions from the contacts and from the semiconductor. Total device resistance can be estimated by treating the device as a network of resistors. The various resistances come from the detailed growth structure of the VCSEL and depend on the current transport path in the devices. A model of a network of resistors, as shown in Fig. 15, was developed for radial current conduction in the p- and n-layers, vertical current conduction through the device aperture, and resistance from the device contacts.

From TLM measurements, we can obtain information on the contact resistances and their corresponding transfer length in the devices and sheet resistance of the semiconductor layers. The transfer length along with contact length gives an estimate of the area of a device contact used to transfer current from the contact to the semiconductor. This effective contact area along with specific contact resistance obtained from TLM measurements will give the resistance contribution of the contact to the total device resistance. For example, the p-contact has an annular design, with an inner radius of 6.5 μm and an outer radius of 8.5 μm. From TLM data, the transfer length for the p-contact was determined to be 1.35 μm. The effective p-contact area can be determined using the simple calculation

$$\pi\left((6.5+1.35)\mu\text{m}\right)^2 - \pi(6.5\ \mu\text{m})^2 = 60.86\ \mu\text{m}^2.$$

This gives a p-contact resistance contribution of 17.09 Ω for a specific p-contact resistance of $1.04 \times 10^{-5}\ \Omega$-cm^2. The n-contact resistance contribution was calculated in a similar manner. The total calculated effective n-contact area is 35.97 μm^2. For a specific contact resistance of $5.56 \times 10^{-6}\ \Omega$-cm^2, this gives an n-contact resistance contribution of 15.46 Ω to the total device resistance. The total contribution of the p- and n-contacts to the device resistance is 32.55 Ω.

Radial conduction can be considered to be the dominant mode of current transport in the device between the device aperture and the contacts. On the p-side of the device, the layers were engineered using varying doping concentrations so that current would spread laterally and then vertically through the aperture for uniform current injection into the active region. Thus, it can prevent the current flowing along the periphery of the aperture, resulting in poor efficiency and preferential pumping of higher order modes. The radial current conduction from the annular p-contact edge to the circular aperture edge will flow from the inner radius of the p-contact to the outer radius of the aperture. The total resistance for lateral current flow in an annulus is

$$R = \frac{\rho_s}{2\pi} \ln\left(\frac{R_o}{R_i}\right)$$

where ρ_s is the sheet resistance and R_o and R_i are the outer and inner radius of the annulus. The semiconductor resistance for lateral conduction from the p-contact to the aperture is then 56.16 Ω. Radial conduction from the n-contact to the aperture can also be handled using the above equation. The sheet resistance measured from TLM data can only be applied for lateral current conduction layers below the n-contact, though. For lateral conduction in layers of the device mesa above the n-contact, the sheet resistance is estimated using the following expression:

$$\rho_s = q\left(\frac{1}{\mu_n N + \mu_p P}\right)$$

where q is the electronic charge, μ is the n-type or p-type carrier mobility denoted by the subscript, and N and P are the electron and hole concentrations, respectively. When considering n-type material (i.e., N $\gg$ P), the second term in the denominator can be ignored. So the resistance due to n-lateral conduction in the device includes a resistance from the n-contact edge to the device mesa edge in series with resistances in parallel from the mesa edge to the aperture edge. The calculated resistances and pertinent information are shown in Table II.

As mentioned before, resistance due to vertical conduction in our VCSEL devices will be small as compared to radial conduction. The current will travel through very thin layers for a total thickness of about $\sim 0.3\ \mu$m. The current is assumed to conduct through a cylinder or a series of disks if you look at layers separately, with a radius of 3.5 μm, as defined by the aperture size. The equation for estimating resistance for current flow through a disk is $R = (\rho d)/(\pi r^2)$, where ρ is resistivity, d is the thickness of the layer, and r is the radius of the aperture. This cylinder model will overestimate the resistance of vertical conduction because the actual shape will be that of an hourglass as created by aperture formation using ion implantation. Table II shows a compilation of the calculated resistances due to the ohmic contacts and to the vertical and lateral current conduction.

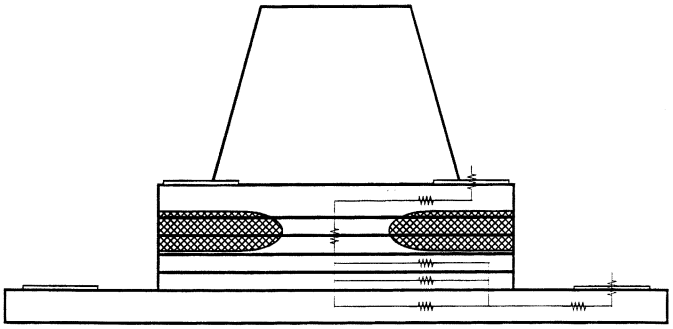

Fig. 15. Model of network of resistors for radial current conduction in the p- and n-layers, vertical current conduction through the device aperture, and resistance from the device contacts.

TABLE II
ESTIMATED RESISTANCES DUE TO THE OHMIC CONTACTS AND TO THE VERTICAL AND LATERAL CURRENT CONDUCTION

$R_{c,n}$	N-contact	15.5Ω
$R_{c,p}$	P-contact	17.1Ω
$R_{rad,n}$	N-side lateral conduction	175.6Ω
$R_{rad,p}$	P-side lateral conduction	56.2Ω
R_{vert}	Vertical conduction through aperture	46.5Ω

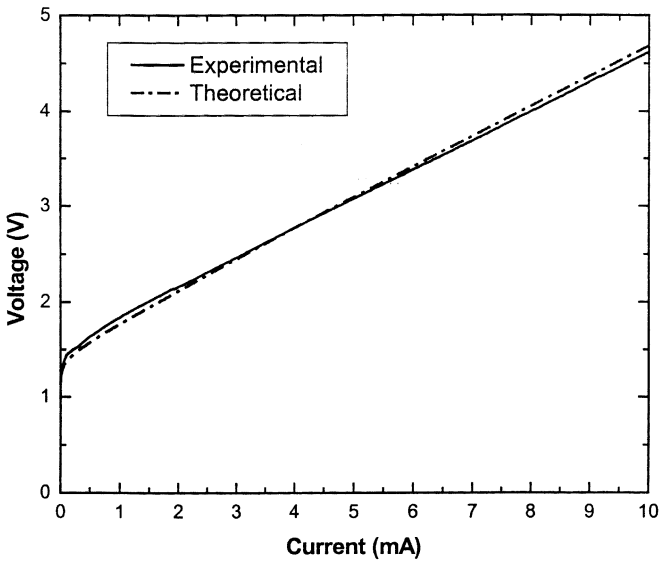

Fig. 16. Comparison of the calculated and experimental I–V characteristics.

Using the calculated resistances, we were able to calculate the expected I–V characteristic from our lasers using the relation $I_F = I_{\rm sat}\exp[q(V_F - R_T I_F)/(mk_BT)]$, where I_F and V_F are the forward bias current and voltage, $A_{\rm act}$ is the area of the aperture, $J_{\rm sat}$ is the saturation current density, R_T is the total series resistance in the device, and m is the diode ideality factor. The value $I_{\rm sat}$ was determined by extrapolating the forward I–V characteristic to the $V = 0$ axis. This value is ∼6e-16 mA. An ideality factor of two was used for this model. This is the value used to describe Shockley–Read–Hall recombination current, which is what we observed for our implanted VCSELs. The total device resistance was determined to be 310.9 Ω using the methods described in the previous sections. Fig. 16 shows a comparison of the calculated and experimental I–V characteristics. There is clearly excellent agreement, indicating the accuracy of our simple model for the resistance components.

V. Thermal Simulations

Good thermal dissipation for the device design is a prerequisite for the high-speed performance. The finite difference method was used to analyze the effect of flip-chip bond design on the thermal characteristics of a TiO_2/SiO_2-based top mirror, implanted-aperture, and lateral current injected 850-nm VCSELs. Fig. 17 shows schematics of the bottom mounted and flip-chip bond VCSEL devices. The active device fabrication steps are identical for these two VCSELs. The only difference is that conventional VCSEL is bottom mounted and the flip-chip bonded VCSEL uses Au-Sn based solder bumps to connect the VCESL to a carrier through its contact pads. The simulation employs three-dimensional finite difference analysis to calculate the temperature $T(r,\theta,z,)$ inside the VCSEL, and nonuniform heat source distribution is considered. This modeling is based on the typical equation of energy balance for cylindrical coordinates (r-, θ-, and z-axes)

$$\rho_{\underline{d}} C_p \frac{\partial T}{\partial t} - k\left[\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right) + \frac{1}{r^2}\frac{\partial^2 T}{\partial \theta^2} + \frac{\partial^2 T}{\partial z^2}\right] = \frac{J^2}{\sigma}$$

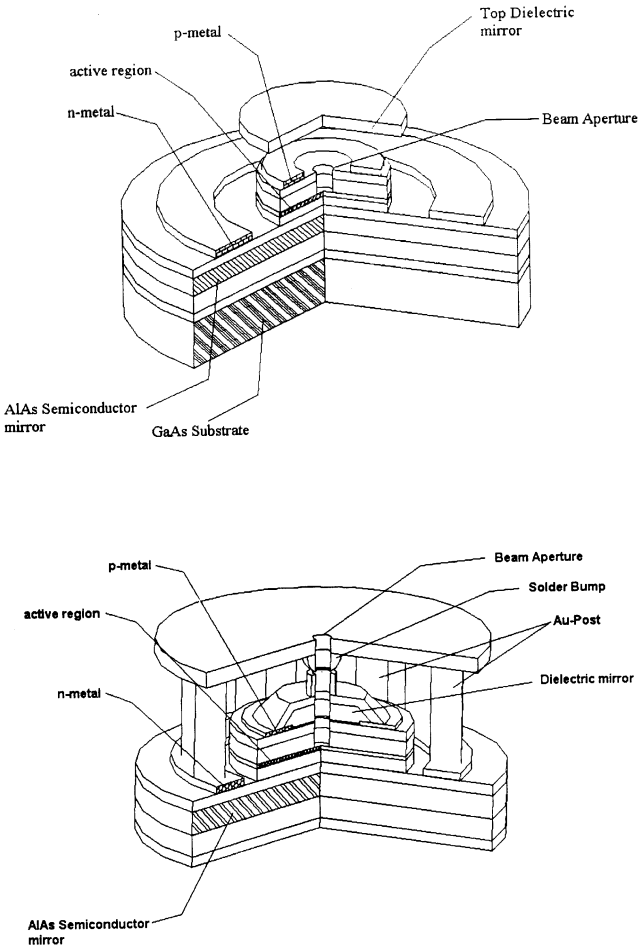

Fig. 17. Schematics of the bottom mounted and flip-chip bond VCSEL devices.

where t is time, ρd is density, C_p is heat capacity, J is current density $[A/cm^2]$, k is thermal conductivity $[W/cm\cdot K]$, and σ is conductivity of each layer. The term on the right side of the energy balance equation corresponds to heat generation quantity per unit volume $[cal/cm^3]$. The quantity of heat generation varies depending on specific regions and layers since current density and conductivity are functions of doping, composition, and geometry of the device. The device dimension and temperature range considered in our case are very small; therefore, it is reasonable to assume the heat transfer through heat convection can be ignored. The heat transfer is dominated by heat conduction through the semiconductor, metal contacts, and the air surrounding the device.

The main heat generation (85%) in the device occurs due to Joule heating, the resistance of semiconductor layers. Joule heating is giving by

$$W(r,\theta,z) = \rho(r,\theta,z)j^2(r,\theta,z)$$

where j is the current density flowing in the device and ρ is the electrical resistivity of the materials for the VCSEL layers. Based on the VCSEL resistance model in the previous section, the resistances of metal contacts, epilayers in terms of the electrical current flow directions (vertical or lateral), and the Joule heat generations were estimated for each unit cell in our model

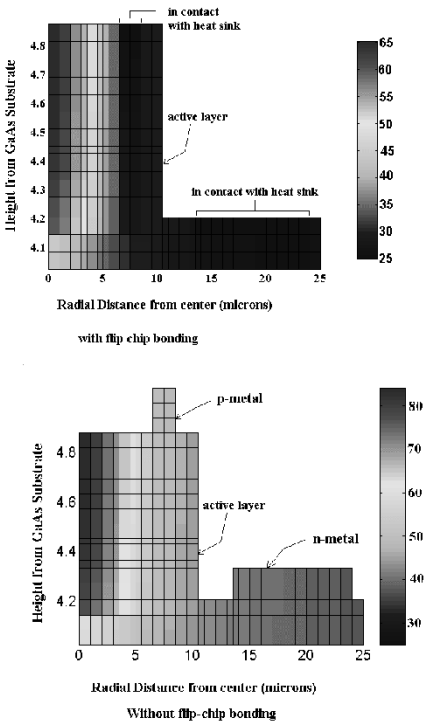

Fig. 18. Two-dimensional temperature distribution of VCSEL with and without flip-chip bonding.

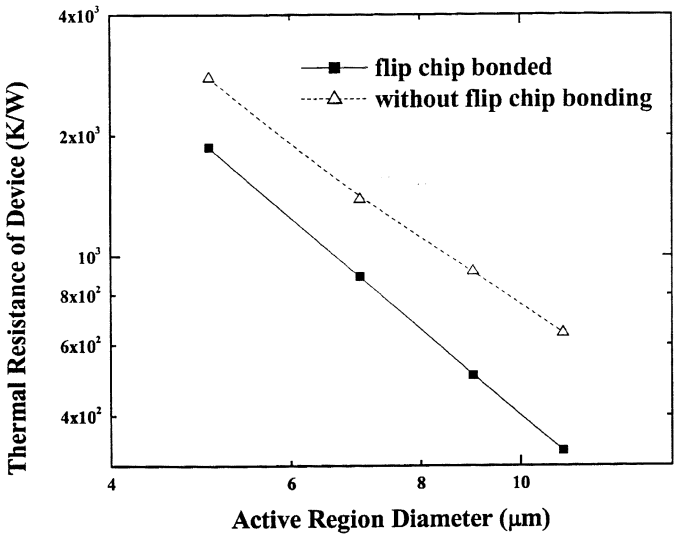

Fig. 19. Temperature at the active region for different levels of input current.

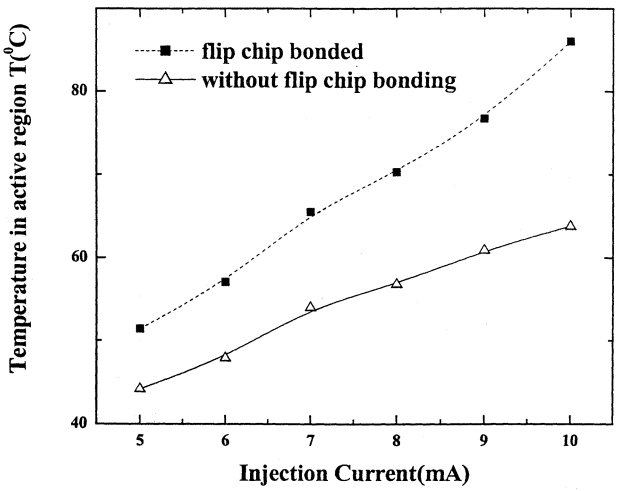

Fig. 20. Thermal resistance of a VCSEL as a function of the aperture diameter.

[28]. The other major heat source (5%) is nonradiative recombination in the active region. Nonradiation recombination is governing by Auger recombination and Shockley–Read–Hall recombination, this portion of the heat generation was determined from the measured LIV characteristics of the laser diode and the estimated Joule heat generations.

Two-dimensional temperature distribution of VCSEL with and without flip-chip bonding is illustrated in Fig. 18. The maximum temperature rise is 60°C for the structure without flip-chip bonding and 42°C for the flip-chip bonded VCSEL. The result is in excellent agreement with the measurement temperature rise of 1.96°C/mS for 30-mW input power [29]. The flip-chip bonded structure differs from the other due to the fact that the contact (n and p) acted as heat sinks. The maximum temperature occurred in the core of the cylindrical VCSEL near the top, because the center-top of VCSEL is covered by a dielectric mirror, which has a low thermal conductivity. Fig. 19 illustrated the temperature at the active region at different levels of input current. The temperature difference between a flip-chip bonded device and bottom bonded device increases from 15°C at low current injection level to $> 20\ ^{\circ}$C at high current injection region. This clearly demonstrates the efficiency of heat dissipation of flip-chip bonded device.

Fig. 20 only shows the device thermal resistance in the active region. The dielectric mirror used in our VCSEL is not a good thermal conductor. Thus the higher thermal resistance is expected as compared to a conventional VCSEL with a semiconductor-based mirror. However, with flip-chip design, the heat is directly conducted out to the heat sink through the top of the VCSEL, and the thermal resistance is significantly reduced. The thermal resistance of the flip-chip bonded device shows almost half that in the back-side bonded device. This is consistent with the temperature profiles of the devices showing that the heat dissipation is much more efficient in the flip-chip bonded device. The thermal resistance is also expected to be lower than that of a normal semiconductor-mirror-based bottom mounted VCSEL. The thermal resistance R monotonically decreases as the active region diameter increases. In the model, we assume constant current for different diameters of the active layer. The larger diameter device has less current density; therefore, the thermal resistance is smaller. We also simulated the effect of active layer thickness on thermal resistance, which is quite minimal and can be ignored.

The above simulation results are based on a steady-state solution, which describes only the thermal equilibrium reached. To investigate the temperature's rising while device is turning on, a dynamical modeling was investigated. Fig. 21 shows the temperature variation as a function of time in the active region. The simulation result shows the temperature's rise due to internal heat generation is significant (maximum temperature is around 60°C at 1–10 mA). The temperature profile reached steady state

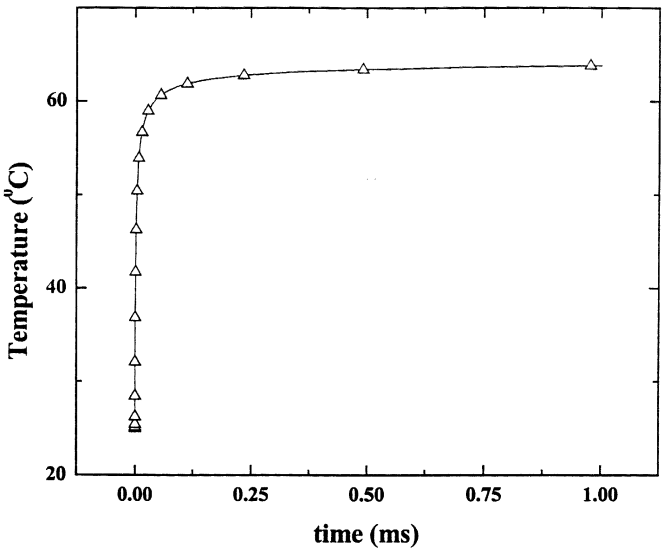

Fig. 21. Light current–voltage characteristic for an 850-nm I^2 VCSEL.

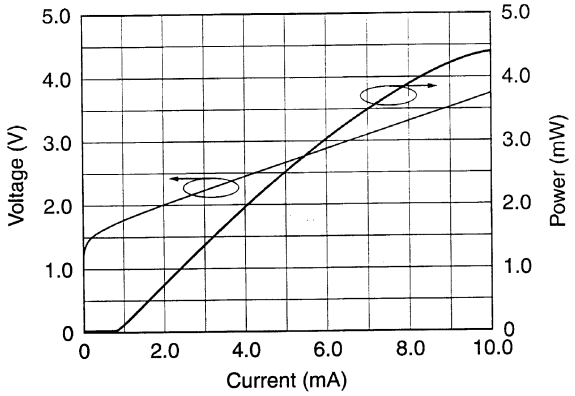

Fig. 22. High-resolution optical spectrum of a VCSEL at an operating current of 4 mA.

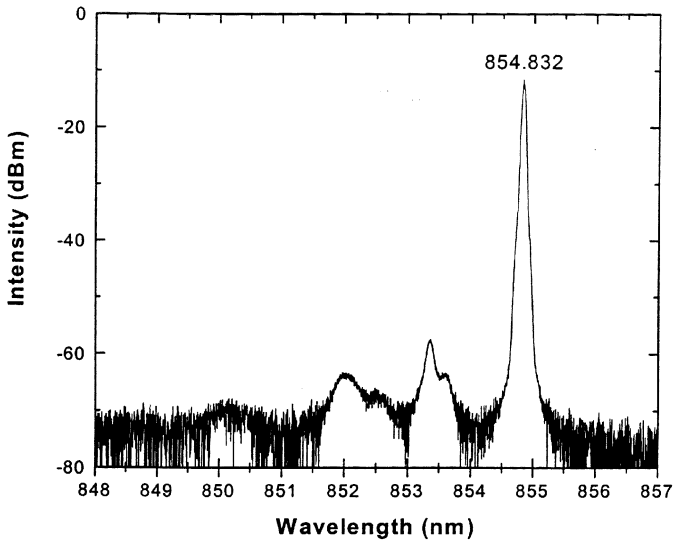

Fig. 23. Multimode CW output characteristics from larger aperture ($8 \times 8\mu m^2$) diodes as a function of device current.

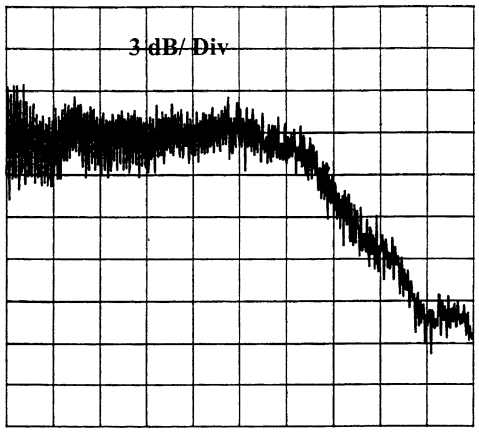

Fig. 24. Small signal measurement of an 850-nm VCSEL.

in the range of a few tenths of milliseconds; however, both small signal and large signal performance of our VCSELs are above 10 Gb/s. As mentioned earlier, the wavelength, peak power, threshold current, and slope efficiency strongly depend on operation temperature of the VCSEL. This means that efficient heat dissipation in the VCSEL is very critical to minimize the shifts of VCSEL characteristics.

VI. Device Results

The light current–voltage characteristic for an 850-nm I^2 VCSEL is given in Fig. 22. The current aperture is 7 μm and a second, deep implant into selected areas of the n-LCI layer is used to reduce the device capacitance. An output mirror reflectivity of 99.5% was used. A threshold current of 0.8 mA and threshold voltage of 1.695 V was achieved. The slope efficiency is 0.47 mW/mA and the differential resistance is 210 Ω.

A high-resolution optical spectrum of a VCSEL at an operating current of 4 mA is shown in Fig. 23. This spectrum was recorded with an ANDO model AQ6317 optical spectrum analyzer. The spectral resolution is 0.01 nm. This particular device is multimode. The relative intensity difference between the fundamental mode and the higher order modes is less than 30 dB above an operating current of 2 mA. The fundamental mode is located in the vicinity of 852.0–852.5 nm, with the two peaks corresponding to the polarization splitting. Higher order modes are evident at shorter wavelengths.

Small-signal analysis of this laser demonstrated a 3-dB modulation frequency exceeding 11.5 GHz, as illustrated in Fig. 24. These measurements were limited by the performance of the test equipment. We used an HP model 8722ES network analyzer and a Picometrix 10-GHz receiver. A higher frequency response detector is required to further determine the limits to the modulation response.

Large-signal digital modulation experiments were performed using a 12-Gb/s bit error rate filter and 26-GHz screening oscilloscope. Fig. 25 shows an eye diagram generated of a VCSEL through 300-m optical fiber at 12 Gb/s by a pseudorandom bit sequence (PRBS) of $2^{31}-1$ and confirms the excellent high-speed performance of 850-nm VCSELs. The bit error rates are

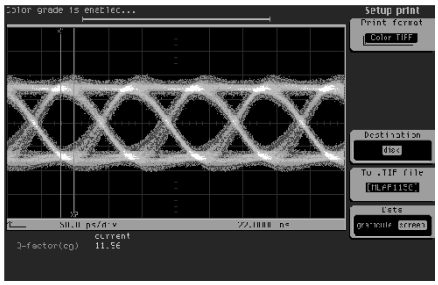

Fig. 25. An eye diagram generated at 12 Gb/s by a PRBS of $2^{31}-1$.

less than 10^{-13} at 10 Gb/s. The characteristics compare well with oxide-confined VCSEL's and emphasize the promise of the implant process for aperture formation [13], [14].

VII. Conclusion

Process integration and optimization of high-speed implant-apertured index-guide lateral current-injection dielectric-mirror GaAs quantum-well VCSELs have been demonstrated. Oxygen and helium implantation were used for aperture definition and extrinsic capacitance reduction, respectively. A negative resist liftoff and SF_6-based dry etch process were developed to pattern the SiO_2/TiO_2 dielectric mirrors. AuBe/Pt/Au and Pd/Ge/Pt/Au were employed for p- and n-ohmic contacts, respectively, and low specific contact resistivities were obtained for both contacts. A resistance model was developed to optimize the epilayer structure to minimize the parasitic resistance. A thermal analysis was also investigated to optimize the heat dissipation with a flip-chip bond configuration. Small signal modulation bandwidths up to 11.5 Gb/s and an eye diagram generated at 12 Gb/s by a pseudorandom bit sequence of $2^{31}-1$ of GaAs/AlGaAs-based 850-nm VCSELs fabricated with this process integration were achieved.

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